

Combinational Logic Circuits using Aldec Active-HDL 9.2 and Xilinx ISE 14.2

Aldec Active-HDL software can be used to generate and simulate designs using VHDL. Aldec is not targeted to any one specific manufacturer of programmable logic devices (PLDs) or Field Programmable Gate Arrays (FPGAs), but produces a vhd file that can be implemented (or “synthesized”) into various devices using various synthesis tools. We will use Xilinx ISE WebPack 14 to synthesize our design into the Xilinx Spartan-3E FPGA. This FPGA is conveniently mounted on an FPGA board called by BASYS2 by Digilent. The BASYS2 provides easy access to input and output pins; slide switches and pushbutton switches for inputs; LEDs and 7-segment displays for outputs; USB2, video and PS2 ports; and PMOD connectors for interfacing with other devices.

Aldec Active-HDL

- Define inputs and outputs
- Describe functional operation
- Create testbench and test design
- Generate truth tables and waveforms
- Compile and produce vhd file

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vhd file (e.g., MyFile.vhd)

Xilinx ISE

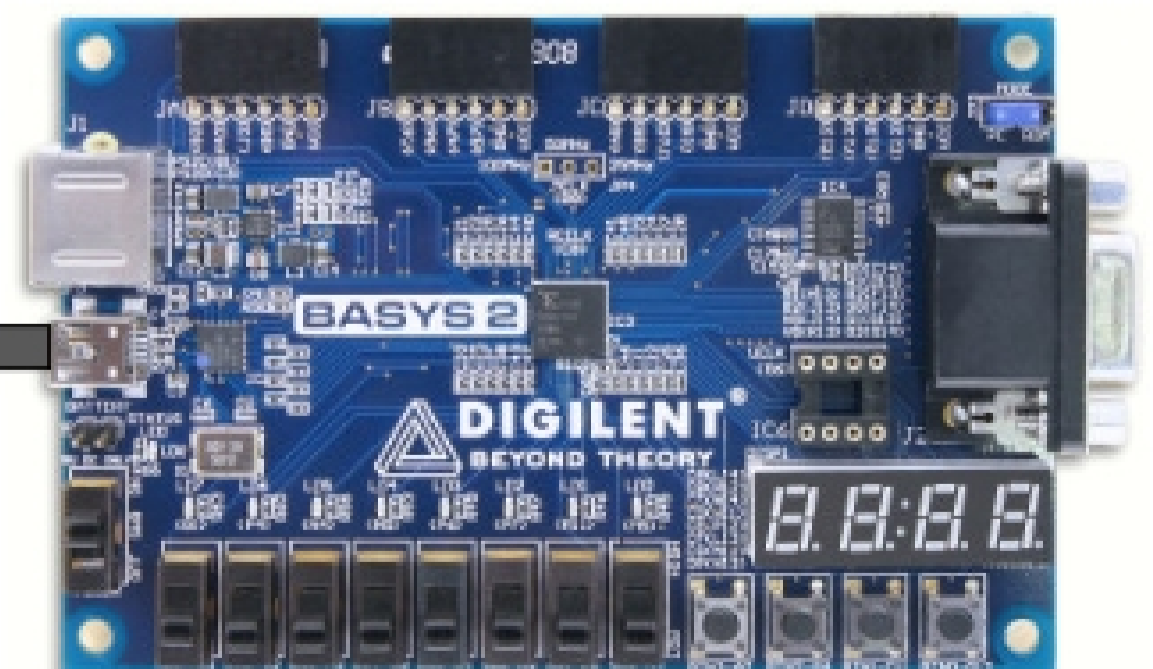
- Specify FPGA Package (Xilinx Spartan 3E, etc)
- Assign signals to pins
- Implement design
- Generate reports
- Produce bit file

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bit file (e.g., MyFile.bit)

Digilent Adept

- Program to download bit files into Digilent devices
- Identify FPGA board: BASYS2
- Identify bit file
- Download (Program the FPGA)

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**USB2
cable**

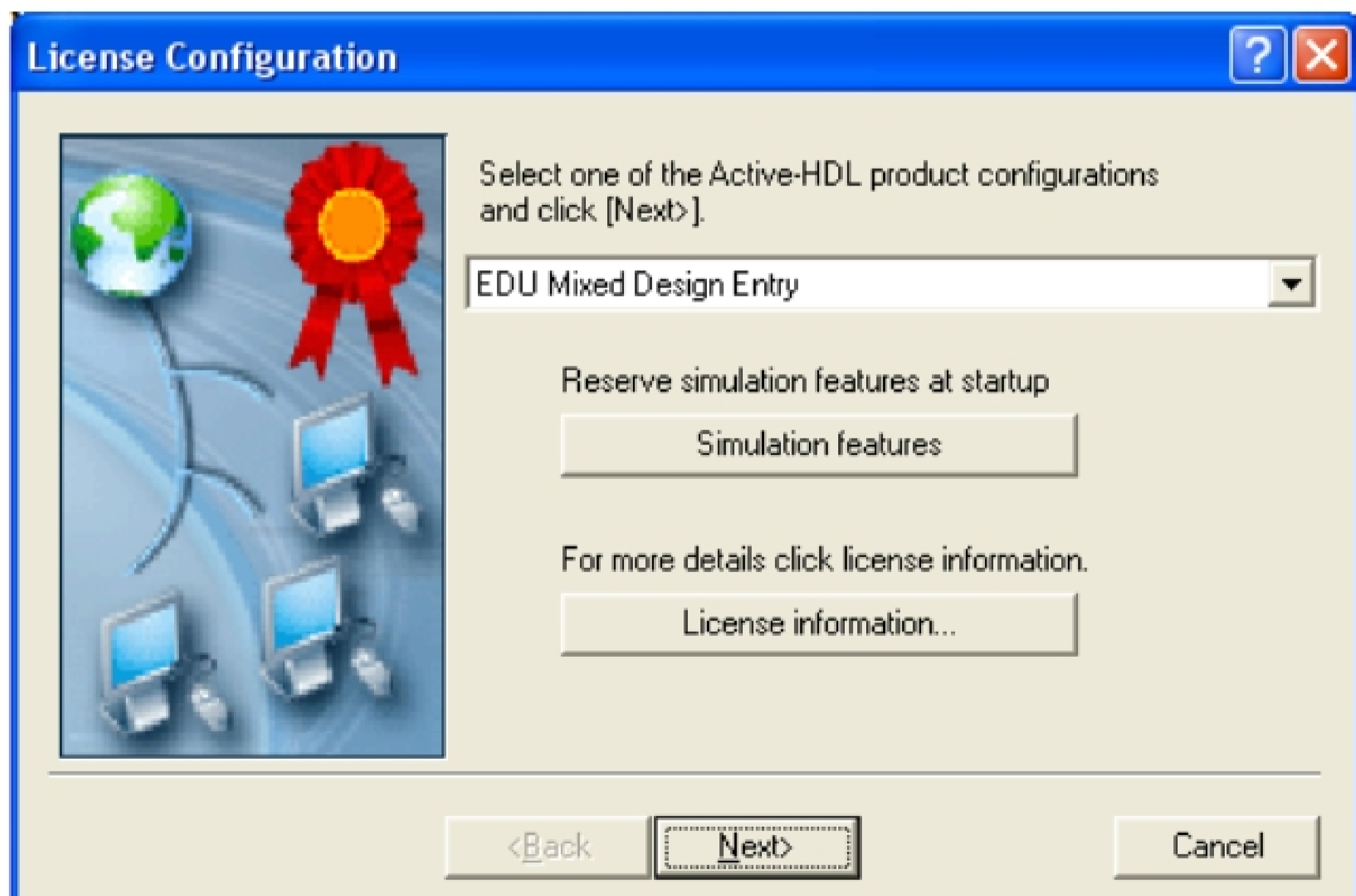


This tutorial will guide you through:

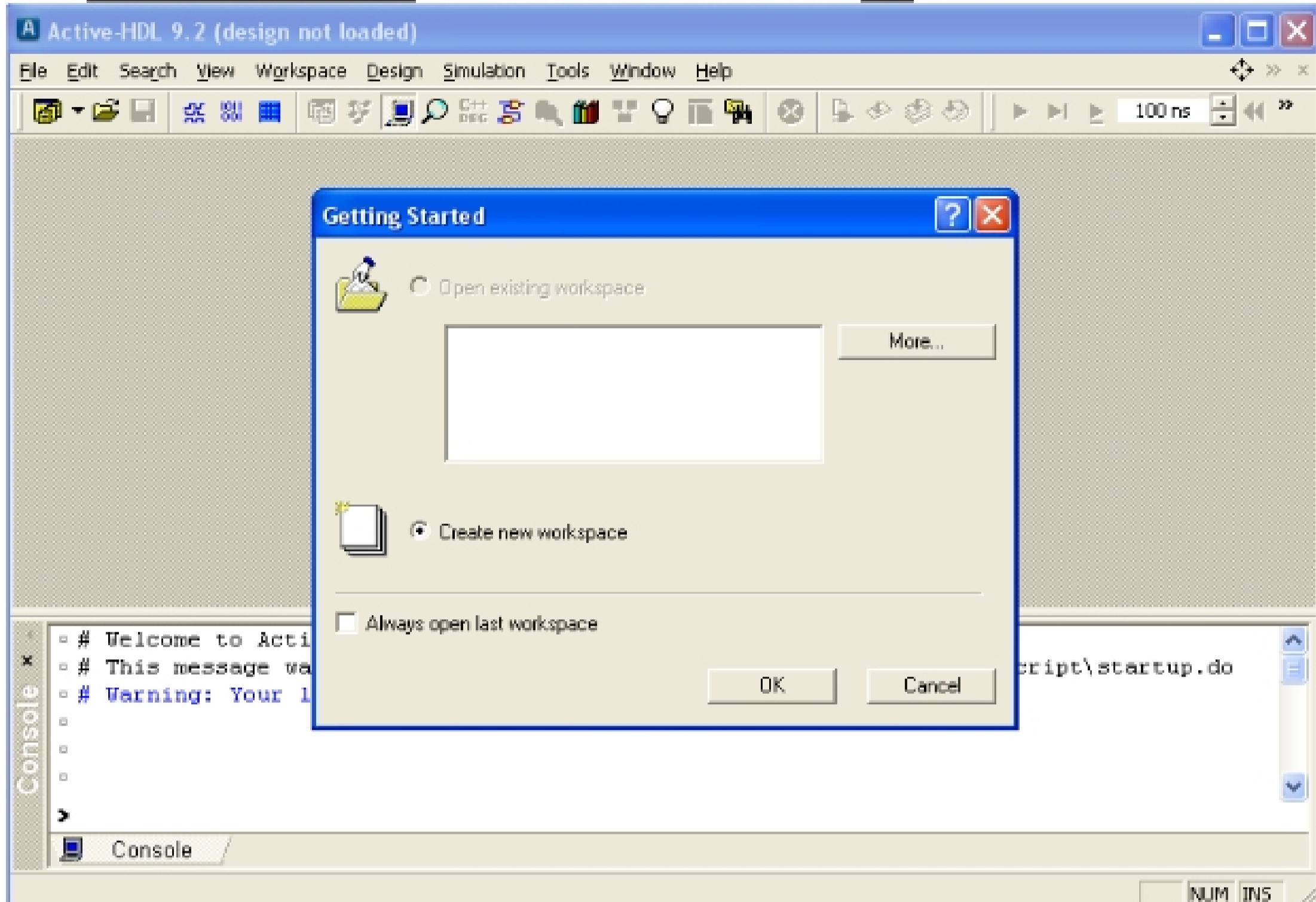
- Using Aldec Active-HDL software to:
 - Enter and compile VHDL code for a simple combinational logic circuit
 - Generate a testbench and simulate the design
 - Produce truth tables and waveforms verifying proper operation
- Using Xilinx ISE software to:
 - Specify the type of FPGA to be programmed
 - Assign input and output signals to FPGA pins
 - Implement the design (producing a bit file)
 - Generate reports
- Using Digilent Adept software to:
 - Select the board to be programmed: Digilent BASYS2 FPGA board
 - Select the bit file to be used
 - Program the FPGA board
- Testing the design on the BASYS2 board.

1. Creating a Project with Aldec Active-HDL

- Launch Aldec Active-HDL 9.2
- The screen below should appear. Select Next.



- Select **Create new workspace** as shown below and then select **OK**



- Enter a name for the workspace (**Ex1** was entered below), change the location of the workspace folder (or use the default as below), and select **OK**. Note that the name for the project workspace, VHDL entity (to be entered later), and architecture (to be entered later) should be the same. *Use letters, numbers and underscores only for filenames.*

