Electronic Circuits Laboratory
EE462G
Lab #6

Using NMOS Transistors to Build Logic Gates

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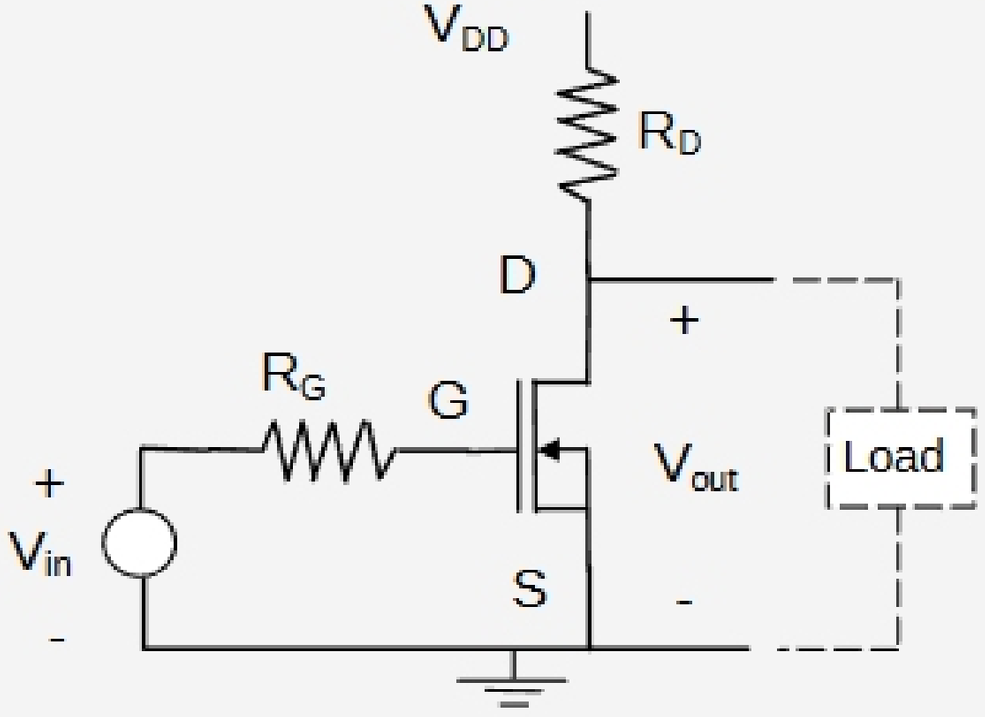
Logic Device Nomenclature

5-Volt Positive logic: Logic gate circuitry where a 5V level corresponds to logic 1 and 0V level corresponds to logic 0.

- **Truth Table:** Input-output description of gate in terms of logic symbols.
- $\mathbf{V_{IL}}$**:** Highest input voltage guaranteed to be accepted as a logic 0.
- $\mathbf{V_{IH}}$**:** Lowest input voltage guaranteed to be accepted as a logic 1.
- $\mathbf{V_{OL}}$**:** Highest logic-0 output voltage produced (given inputs are consistent with $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$).
- $\mathbf{V_{OH}}$**:** Lowest logic-1 output voltage produced (given inputs are consistent with $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$).

FET Operation as a Logic Device

Input values will change between 0 volts ($V_{GS} < V_{tr}$) and 5 volts ($V_{GS} > V_{DS}+V_{tr}$). Thus, the NMOS transistor will operate primarily in the cutoff and triode regions. The circuit below represents a logic inverter.



Three Regions of Operation:

Cutoff region ($V_{GS} \leq V_{tr}$)

Triode region ($V_{DS} \leq V_{GS} - V_{tr}$)

Saturation ($V_{GS} - V_{tr} \leq V_{DS}$)