Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Circuits & Electronics
Spring 2005

Lab #1: Thevenin/Norton Equivalents & Logic Gates

Introduction

This lab has two independent parts, each with pre-lab, in-lab and post-lab exercises. The first part explores the characterization of a network by its Thevenin and Norton equivalents. The second part explores the static behavior of logic gates constructed with n-channel MOSFETs and resistors. You should complete the pre-lab exercises in your lab notebook before coming to lab. Then, carry out the in-lab exercises on your assigned lab day between February 28 and March 4. After completing the in-lab exercises, have a TA or LA check your work and sign your lab notebook. Finally, complete the post-lab exercises in your lab notebook, and turn in your lab notebook during recitation on Wednesday March 9.

Pre-Lab Exercises

Pre-Lab Exercises 1-1 and 1-2 explore the characterization of a network by its Thevenin and Norton equivalents. Pre-Lab Exercises 1-3 through 1-5 explore the static behavior of logic gates.

(1-1) Determine the Thevenin and Norton equivalents of the network shown in Figure 1 as viewed at its port.

(1-2) Evaluate the Thevenin and Norton equivalents of the network for the following values: $V = 5$ V; $R_1 = 50\ \Omega$; $R_2 = 2.2$ kΩ; $R_3 = 1.5$ kΩ.

(1-3) Figure 2 shows a NOT gate, or inverter, a NOR gate and a NAND gate constructed from n-channel MOSFETs and 1 kΩ resistors. The figure also shows a switch-resistor model for the n-channel MOSFET. Using the switch-resistor model, compute v_{OUT} for all three gates. In doing so, consider all combinations of input voltages; an input voltage may be either above or below the MOSFET threshold voltage v_{T}. In each case, evaluate v_{OUT} assuming $R_{\mathrm{DS-ON}} = 4\ \Omega$. Summarize your results for each gate in a table.

(1-4) Figure 3 shows a combinational logic circuit. Determine the input-output truth table for this circuit.

(1-5) Draw the circuit diagram for the combinational logic circuit shown in Figure 3 using the

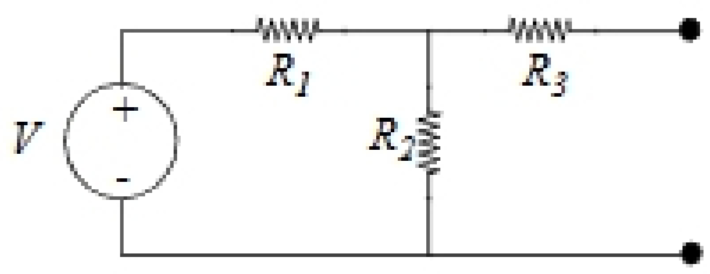

Figure 1: source-resistor network for Pre-Lab Exercises 1-1 and 1-2.

gates shown in Figure 2.

In-Lab Exercises

In-Lab Exercises 1-1 through 1-3 explore the characterization of a network by its Thevenin and Norton equivalents. In-Lab exercises 1-4 through 1-9 explore the static behavior of logic gates.

(1-1) Construct the network shown in Figure 4. However, before connecting the signal generator to the remainder of the network, set its output voltage to a constant 5 V, and check this output with the multi-meter. Note that the network is the same as that shown in Figure 1, with the function generator serving as both the voltage source and resistor R_1. *Note that the function generator has two modes for displaying voltage: 50 Ω and High Z. Make sure that your function generator is set to the High Z mode. Press [Shift] and then [Enter] to get to the menus. Using the dial, switch to menu D, the SYS MENU. Next press the down arrow twice. Use the dial to switch to HIGH Z. Then press [Enter] to save.*

(1-2) Measure the open-circuit voltage and short-circuit current of the network with the multi-meter. Note that the multi-meter is itself a near open circuit when used as a voltmeter, and a near short circuit when used as an ammeter. Therefore, the direct connection of the multi-meter across the port implements the proper measurement in both cases. Your results from Pre-Lab Exercise 1-2 should show that both measurements are within the safe range for the multi-meter.

(1-3) Connect a resistor across the port of the network and measure the port voltage v with the multi-meter. Do so for resistors having resistances of 560 Ω, 1 kΩ and 2.2 kΩ.

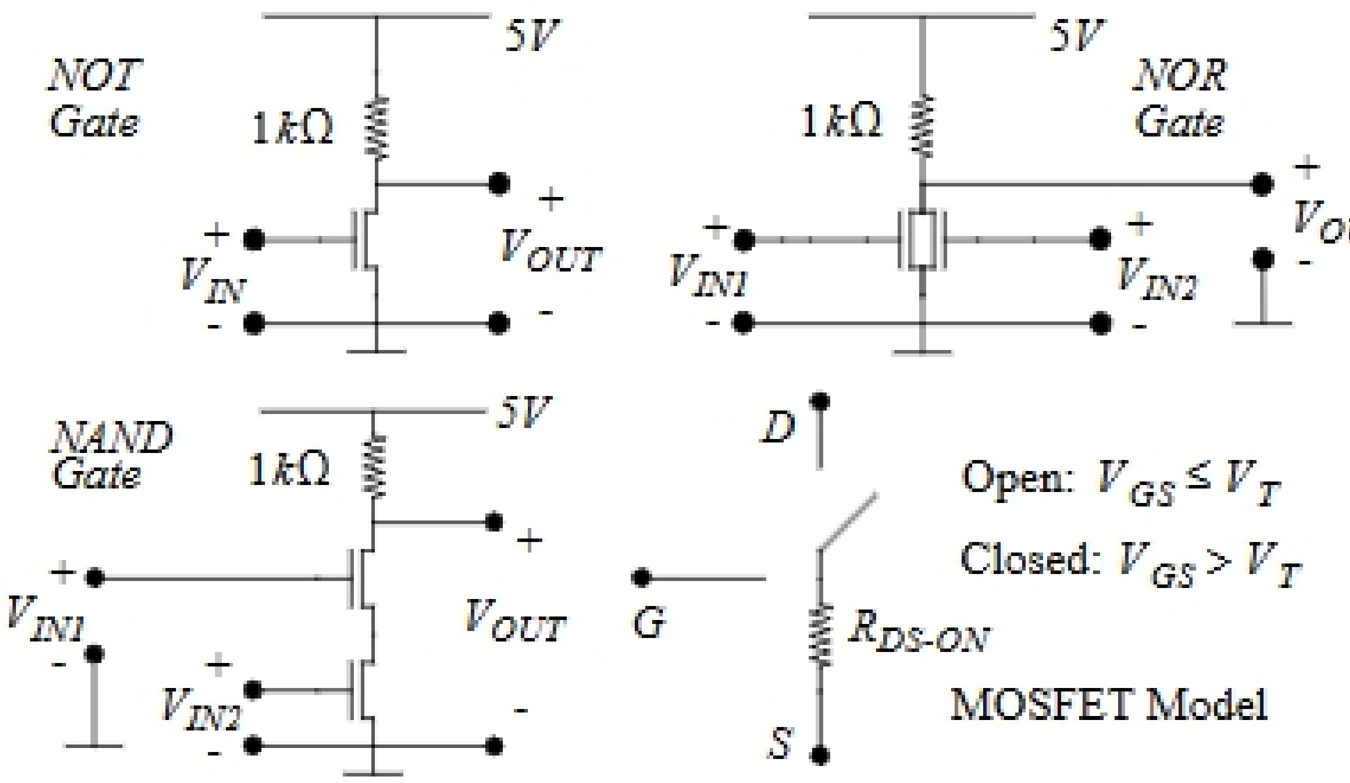

Figure 2: a NOT gate, a NOR gate, a NAN gate, and the switch-resistor MOSFET model.

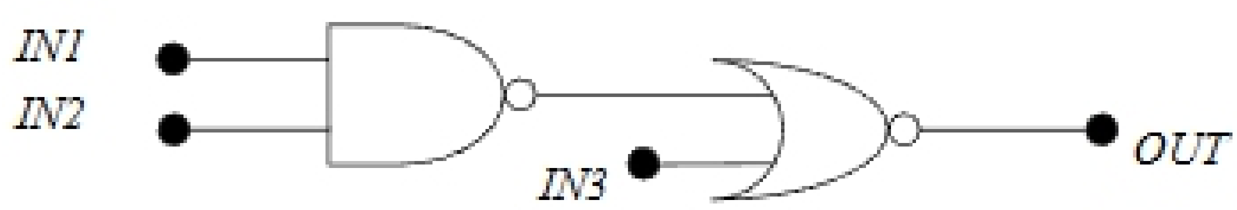

Figure 3: combinational logic circuit for Pre-Lab Exercises 1-4 and 1-5.

(1-4) Construct the circuit shown in Figure 5 to measure the threshold voltage of the MOSFET. The MOSFET should be labeled "2N7000", and its pin assignments are given in the attached data sheet. Use the multi-meter to measure v_{GS} and the oscilloscope to measure v_{DS}, and set the signal generator to provide a constant output. With v_{GS} at 0 V, v_{DS} should be at 5 V. Gradually increase v_{GS} until v_{DS} starts to fall. The value of v_{GS} at which this occurs is v_T. *Caution: avoid handling the MOSFET by its leads because it can be damaged by static electricity. Also, be careful not to reverse the MOSFET leads when constructing the circuit.*

(1-5) Beginning with the circuit shown in Figure 5, disconnect the 1 kΩ resistor and the oscilloscope from the MOSFET drain. With v_{GS} at 5 V, measure R_{DS} with the multi-meter. This resistance is R_{DS-ON} for $v_{GS} = 5$ V; note that the multi-meter supplies a very small voltage when used as an ohmmeter.

(1-6) Construct the NOT gate from Figure 2 and connect its input to a switch and 10 kΩ resistor as shown in Figure 6. For both switch positions, that is for both logic input levels to the gate, measure v_{OUT} with the multi-meter.

The switch pack and the 10 kΩ resistor array have been chosen to simplify the wiring of the switches to their associated resistors. Specifically, the switch pack can be placed in the protoboard so that one side is on a common ground strip and each pin on the other side is on a separate trace. Then, the resistor pack can be inserted into the protoboard along side the switch pack so that separate resistors connect to each switch. Finally, the common pin of the resistor pack can be connected to the 5 V power supply through a single wire. *Caution: the switch-pack pins are fragile, and they can also pop out of the protoboard.*

(1-7) Construct the NOR gate from Figure 2. As for the NOT gate shown in Figure 6, connect

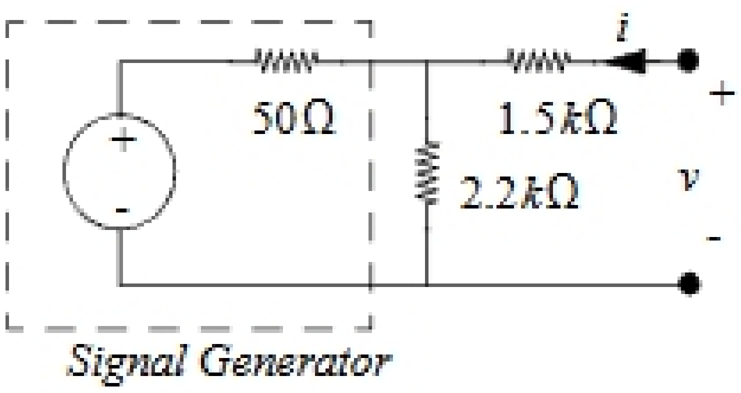

Figure 4: experimental source-resistor network.

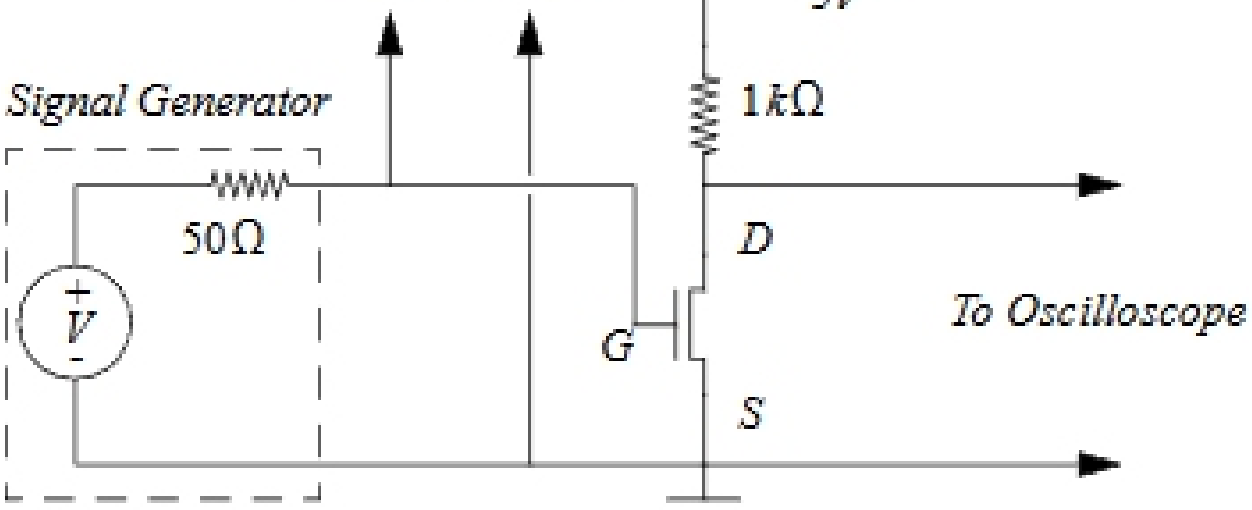

Figure 5: circuit to measure v_T.