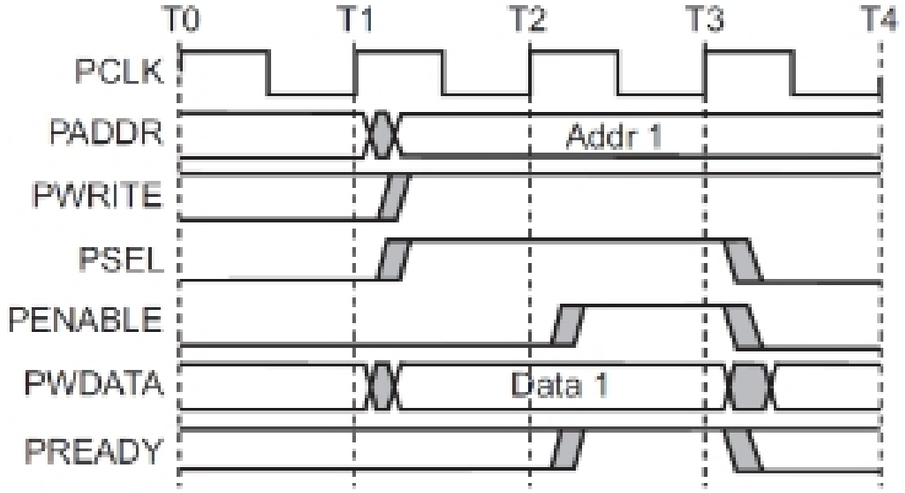
EECS 373
Design of Microprocessor-Based Systems



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Lecture 5: Memory and Peripheral Busses
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Announcements: get started on the simulator!

A6.7.119 STR (immediate)

Store Register (immediate) calculates an address from a base register value and an immediate offset, and stores a word from a register to memory. It can use offset, post-indexed, or pre-indexed addressing. See *Memory accesses* on page A6-15 for information about memory accesses.

```
1  #include "../cortex_m3.h"
2
3  int str3(uint32_t inst) {
4  .       uint8_t rd = (inst & 0x700) >> 8;
5  .       uint16_t immed8 = inst & 0xff;
6
7  .       uint32_t sp = CORE_reg_read(SP_REG);
8  .       uint32_t rd_val = CORE_reg_read(rd);
9
10 .       uint32_t address = sp + (immed8 << 2);
11 .       if ((address & 0x3) == 0) {
12 .       .       write_word(address, rd_val);
13 .       } else {
14 .       .       CORE_ERR_invalid_addr(true, address);
15 .       }
16
17 .       DBG2("str r%02d, [sp, #%d * 4]\n", rd, immed8);
18
19 .       return SUCCESS;
20 }
21
22 void register_opcodes_str(void) {
23 .       // str3: 1001 0<x's>
24 .       register_opcode_mask(0x9000, 0xffff6800, str3);
25 }
```

Encoding T1 All versions of the Thumb ISA.

STR<c> <Rt>, [<Rn>{,#<imm5>}]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	imm5					Rn			Rt		

```
t = UInt(Rt);  n = UInt(Rn);  imm32 = ZeroExtend(imm5:'00', 32);
index = TRUE;  add = TRUE;  wback = FALSE;
```

Encoding T2 All versions of the Thumb ISA.

STR<c> <Rt>,[SP,#<imm8>]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	Rt			imm8							

```
t = UInt(Rt);  n = 13;  imm32 = ZeroExtend(imm8:'00', 32);
index = TRUE;  add = TRUE;  wback = FALSE;
```

Outline

- Minute quiz
- Announcements
- Memory and Memory-Mapped I/O
- Bus Architectures
- ARM APB
- ARM AHB-Lite