



# EECS 373

## Design of Microprocessor-Based Systems

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Lecture 7: Interrupts, ARM NVIC  
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"PLEASE FEEL FREE TO INTERRUPT  
IF YOU HAVE A QUESTION."



<http://home.nccomm.com/~avensent/science.html>



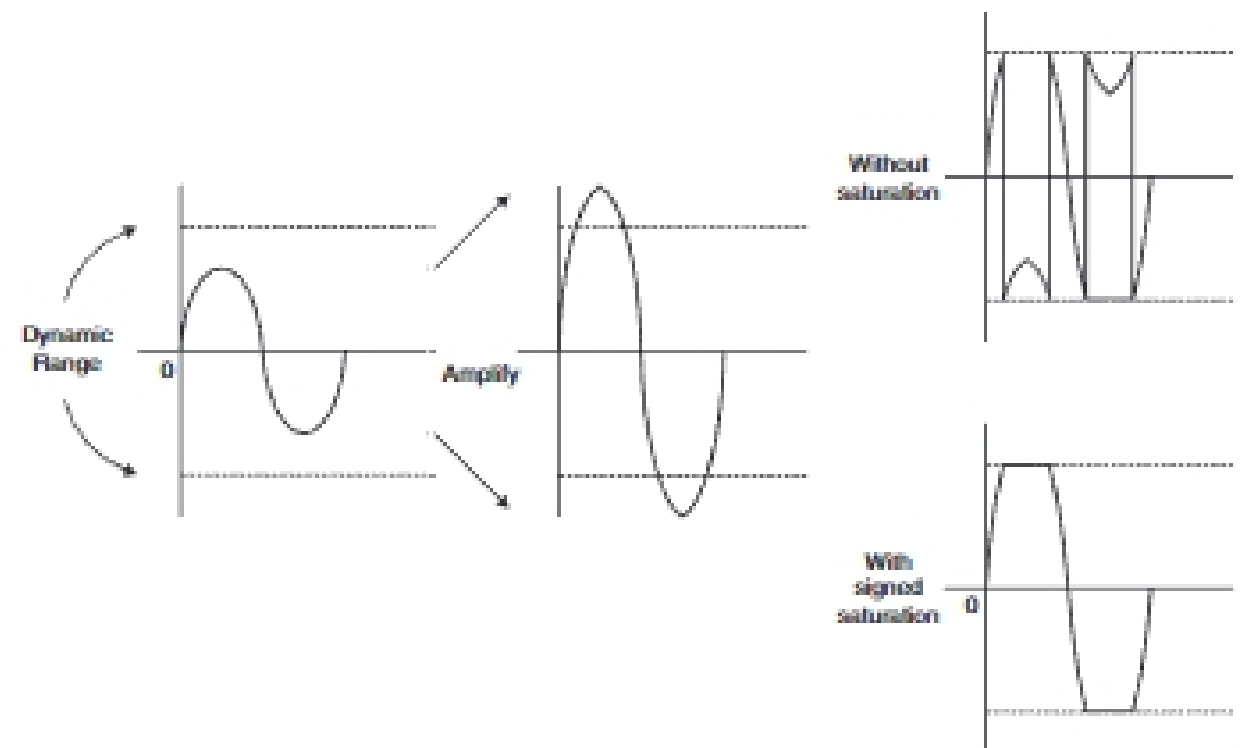
Minute Quiz...

## Recap of the last lecture



- Why is Reset Vector +1?
  - It's an ARM specific thing. The least significant bit in jump instructions indicates the type of instruction at that location (0: for ARM, 1: for Thumb). Since the Cortex-M3 can only execute Thumb2, this will always

## The SAT instruction



From: The Definitive Guide to the ARM Cortex-M3

## Saturating at 32-bit signed value to a 16-bit



```
SSAT.W <Rd>, #<immed>, <Rn>, {,<shift>}  
SSAT.W R1, #16, R0
```

Input (R0)	Output (R1)	Q Bit
0x00020000	0x00007FFF	Set
0x00008000	0x00007FFF	Set
0x00007FFF	0x00007FFF	Unchanged
0x00000000	0x00000000	Unchanged
0xFFFF8000	0xFFFF8000	Unchanged
0xFFFF8001	0xFFFF8000	Set
0xFFFE0000	0xFFFF8000	Set

From: The Definitive Guide to the ARM Cortex-M3

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# Interrupts

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## Generalization of Interrupts



- Merriam-Webster:  
“to break the uniformity or continuity of”
- Informs a program of some external events
- Breaks execution flow
  
- Where do interrupts come from?
- How do we save state for later continuation?
- How can we ignore interrupts?
- How can we prioritize interrupts?
- How can we share interrupts?

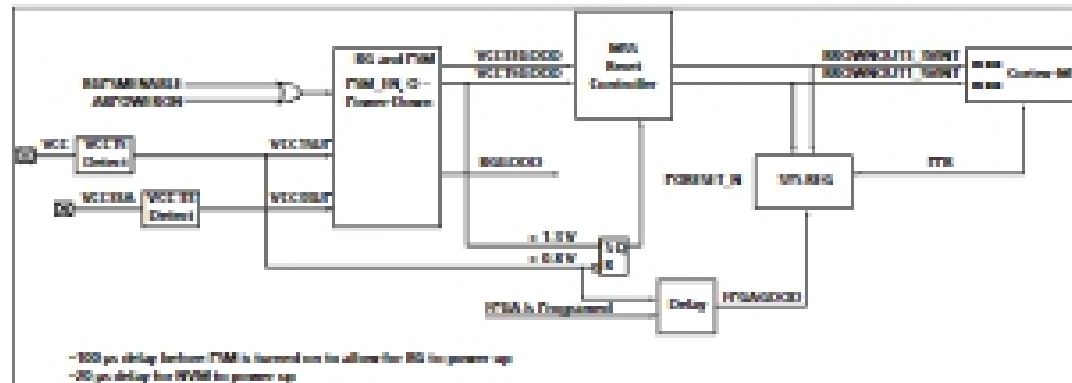
9



How does an embedded system boot?

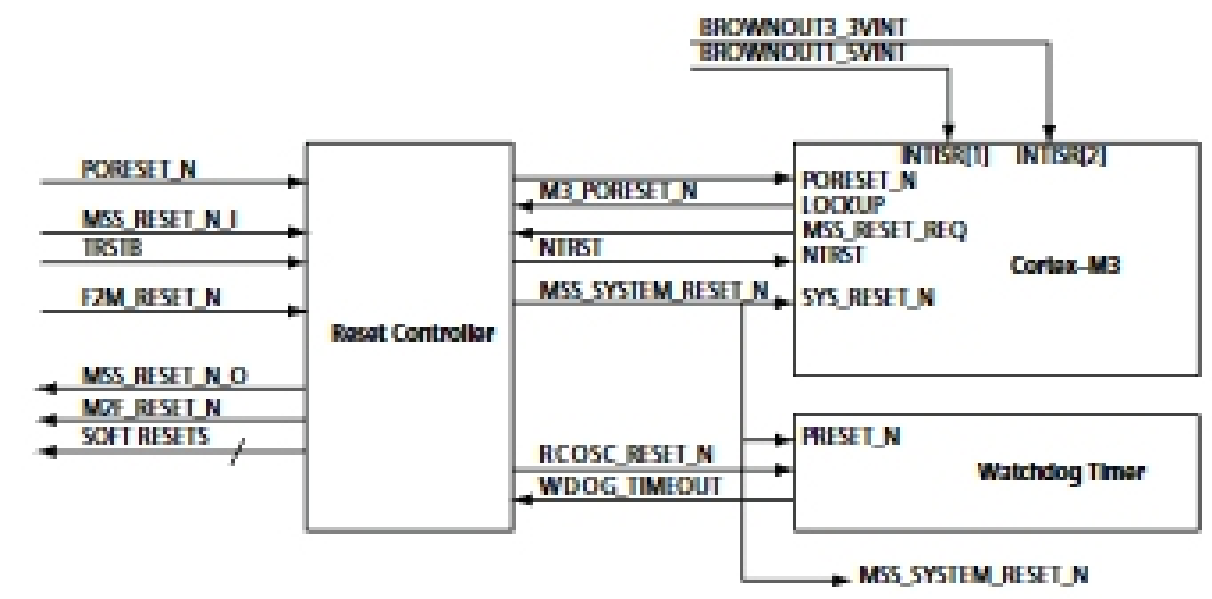
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# The Reset Interrupt



1. No power
2. System is held in RESET as long as  $VCC15 < 0.8V$ 
  - a. In reset: registers forced to default
  - b. RC-Osc begins to oscillate
  - c. MSS\_CCC drives RC-Osc/4 into FSCK
  - d. PORESET\_N is held low
3. Once VCC15GOOD, PORESET\_N goes high
  - a. MSS reads from eNVM address 0x0 and 0x4

# The Reset Interrupt (2)



- The Reset Interrupt is Non-Maskable!

# Interrupt Handling



- On the Cortex-M3
  - Source: Software, Peripheral
  - Controller: Nested Vectored Interrupt Controller (NVIC)
  - MPU: Cortex-M3 Core

# Sources of Interrupts

