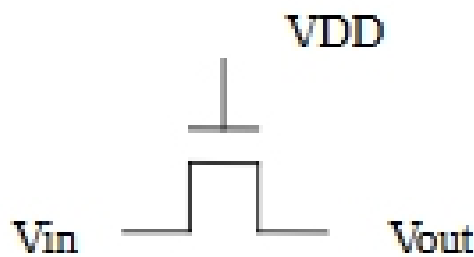
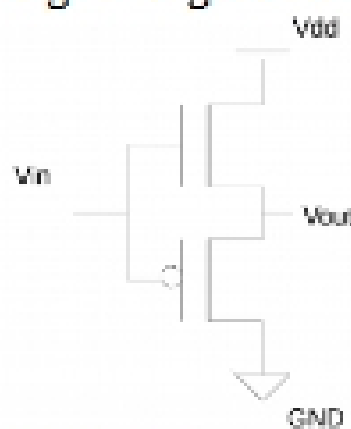


Practice Exam: Midterm, EE466

1. (a) Suppose $V_{DD}=1.2V$ and $V_t=0.4V$. Determine V_{out} for the pass transistor circuit for $V_{in}=0V, 0.6V, 0.9V$ and $1.2V$. Neglect body effect.



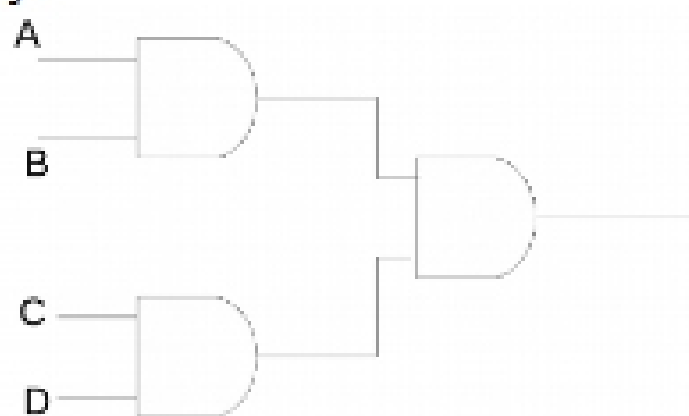
- (b) What is the intended function of the circuit shown below? What is the output voltage swing for this circuit?



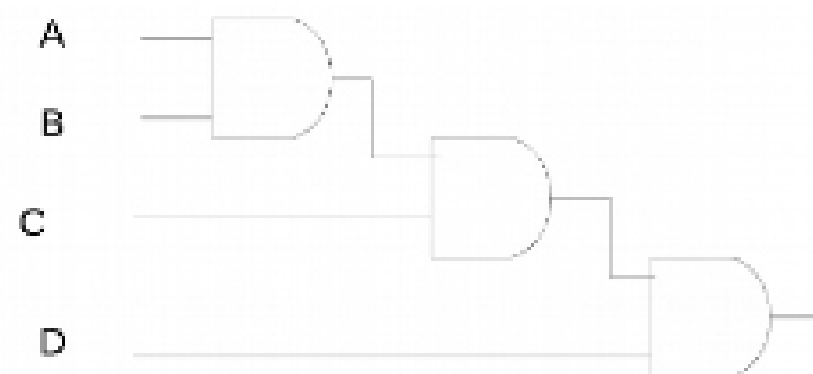
2. (a) Let a 4x inverter have transistors 4 times as wide as a unit sized inverter. What is the input capacitance, logical effort and parasitic delay of the 4x inverter.
 (b) A 3-stage logic path is designed so that the effort borne by each stage is 12,6 and 9 delay units. Can this be improved? Why? What is the best number of stages for this path? What changes do you recommend to the existing design?

3 (a) You are considering lowering V_{DD} to reduce power dissipation in static CMOS gates. You will also scale down V_t proportionally so that the speed is not affected. Will dynamic consumption go up or down? Will static power consumption go up or down?

(b) Which of the following 2 4-input AND gate circuits dissipate less glitching power and why?



tree



chain

4(a) Design an asymmetric 3-input NOR gate that favors a critical input over the others. Choose transistor sizes so that logical effort on critical input is 1.5 What is the logical effort on the non-critical inputs?

(b) Sketch dynamic footed and unfooted 3-input NAND and NOR gates. Label the transistor widths. What is the logical effort of each gate?