The George Washington University
Department of Electrical and Computer Engineering

Fall 2007 **Prof. M.E.Zaghloul**
ECE126 **MIDTERM**

1. a) Consider NMOS transistor. The device is biased with $V_{GS} = 2.2V$, $V_{DS} = 4$ V, and $V_{SB} = 2V$. Compute the value of the aspect ratio (W/L) needed to obtain current flow of $I_D = 100uA$. Use simplified device equation set and the parameters given below

   b) Suppose that the minimum line width in the given technology is 2.5um. Calculate the approximate gate capacitance C_g for the device designed in part a)

   $V_{TO} = =0.8V$ $\gamma = 0.4\ V^{1/2}$ $2|\phi_F| = 0.58$ V $KP = 20\ uA/V^2$

   $C_{OX} = 3.4x10^{-3} pF/(um)^2$

2. a) Explain the types of power dissipation in CMOS circuits

   b) Let the power dissipated by CMOS inverter be approximated by P $=C_L V_{dd}^2$ f. Find the average current consumption by the inverter if $C_L = 0.2$ pf, $V_{dd} = 5.0V$, f = 20MH

3. You are designing a clock distribution network in which it is critical to minimize the skew between local clocks CLK1, CLK, CLK3). You have extracted the RC network as shown in Figure. You noticed the path to LK3 is shorter than CLK1 and CLK2. To compensate you inserted Transmission gate as shown in the Path to CLK3.

a) Write expression for the time constant associated with nodes CLK1, CLK2, CLK3. Assume TG is modeled by R3

b) If R1 = R2 = R4= R5 =R and C1= C2 =C3= C4=C5=C, what value of R3 is required to balance the delay to local clocks.

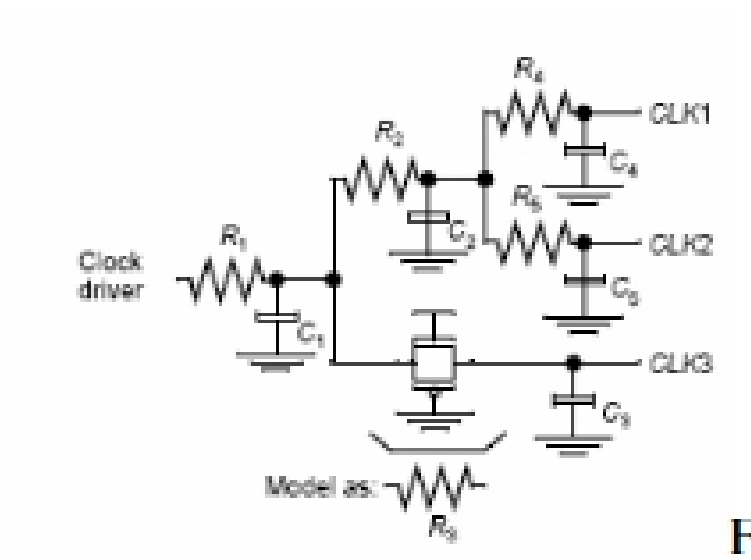

Figure for problem 3

4. Suppose we wish to implement the two logic functions given by F= A+B+C and G = A+B+C+D. Assume both true and complementary signals are available.

   a) Implement these function in dynamic CMOS as cascaded two stages and minimize the number of transistors

   b) Design the circuit as np-CMOS implementation of the same logic function . Does this design display any of the difficulties of part a)

5. Design a Static CMOS circuit to realize the following functions. Illustrate the design using schematic, use module and minimum number of transistors.

   i) XOR

   ii) $Y = A \; XOR \; B \; XOR \; C$

   iii) $F = \overline{(A+B) \cdot (C+D)}$