Lecture 8 - PN Junction and MOS Electrostatics (V)

Electrostatics of Metal-Oxide-Semiconductor Structure (*cont.*)

October 4, 2005

Contents:

1. Overview of MOS electrostatics under bias
2. Depletion regime
3. Flatband
4. Accumulation regime
5. Threshold
6. Inversion regime

Reading assignment:

Howe and Sodini, Ch. 3, §§3.8-3.9

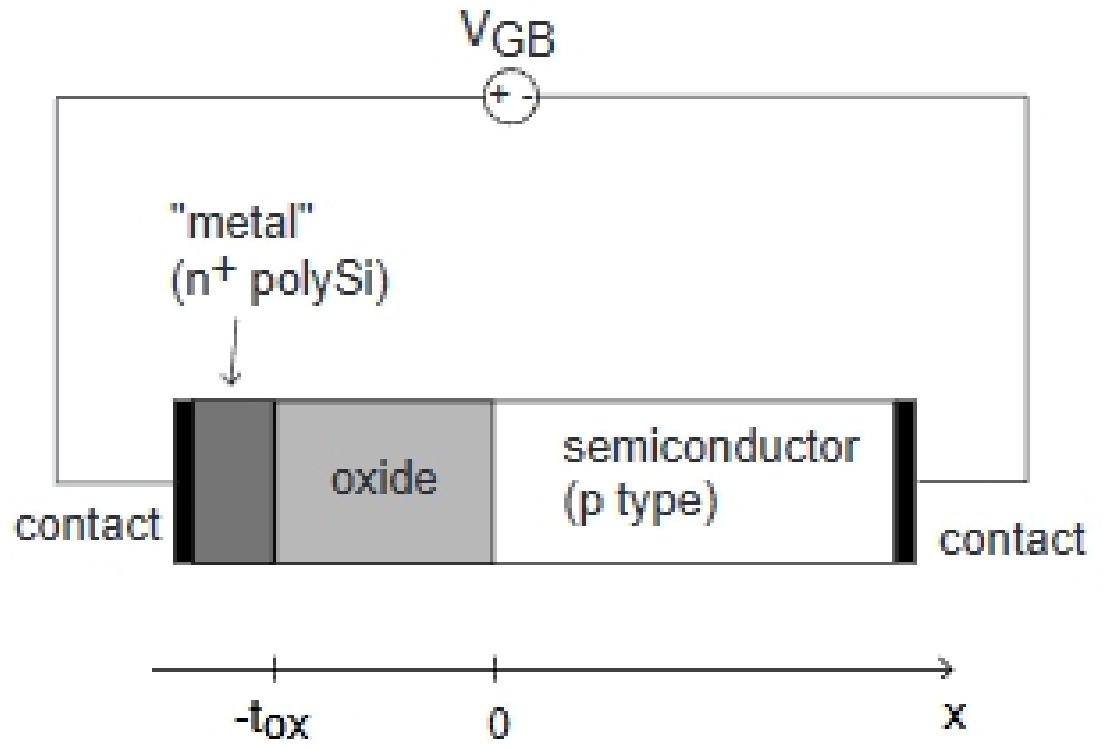
Announcements:

Quiz 1: 10/13, 7:30-9:30 PM, (lectures #1-9); open book; must have calculator.

Key questions

- Is there more than one regime of operation of the MOS structure under bias?
- What does "carrier inversion" mean and what is the big deal about it?
- How does the carrier inversion charge depend on the gate voltage?

1. Overview of MOS electrostatics under bias



Application of bias:

- built-in potential across MOS structure increases from ϕ_B to $\phi_B + V_{GB}$
- oxide forbids current flow $\Rightarrow$
  - $J = 0$ everywhere in semiconductor
  - need *drift=-diffusion* in SCR
- must maintain boundary condition at Si/SiO_2 interface: $E_{ox}/E_s \simeq 3$

How can this be accommodated simultaneously? $\Rightarrow$ *quasi-equilibrium situation* with potential build up across MOS equal to $\phi_B + V_{GB}$