CS152
Computer Architecture and Engineering
Lecture 7

Designing a Single Cycle Datapath

February 18, 2004

John Kubiatowicz (www.cs.berkeley.edu/~kubitron)

lecture slides: http://inst.eecs.berkeley.edu/~cs152/

Review: Sequential Logic + (Non-)blocking assignments

- **Must be careful mixing zero-time blocking assignments and edge-triggering: Probably won't do what you expect when connecting it to other things!**

```
module FF (CLK,Q,D);
   input D, CLK;
   output Q; reg Q;
   always @ (posedge CLK)
      Q <= D;
endmodule // FF
```

Good: Doesn't output until "after edge"

```
module FF (CLK,Q,D);
   input D, CLK;
   output Q; reg Q;
   always @ (posedge CLK)
      Q = #5 D;
endmodule // FF
```

Good: Outputs 5 units "after edge"

Probably Not what you Expect:

- **Hold time of 5 units**
- **glitches < 5 units ignored**

```
module FF (CLK,Q,D);
   input D, CLK;
   output Q; reg Q;
   always @ (posedge CLK)
      #5 Q = D;
endmodule // FF
```

Review: MULTIPLY HARDWARE Version 3

- 32-bit Multiplicand reg, 32-bit ALU,
  64-bit Product reg (shift right), (0-bit Multiplier reg)