

ECE 126 – NAND Gate Tutorial: Mixed Signal Simulation: Using Verilog as Input Stimulus

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Objectives:

- Create a verilog test bench for a 2-input NAND gate
- Use verilog to verify output from a 2-input NAND gate
- Use the Cadence configuration hierarchy editor tool

Assumptions:

- Student has completed the Inverter Tutorial on Mixed Signal Simulation w/ Verilog
- Student has a basic familiarity with verilog
- Student is familiar with simulating off the 'extracted view' of a layout

Introduction:

Up to this point you have used "pulses" and "dc sources" in your test benches to test your Cadence schematics and layouts. In this lab you will learn to create and use a verilog 'source' to test your Cadence schematics and layouts. This will enable you to create more complex test-benches for your final project.

LAB SETUP:

1. *Ensure you have setup your environment as specified in the Inverter Tutorial on Mixed Signal Simulation w/Verilog*
2. *Start Cadence*

NOTE: Many screenshots are omitted from this tutorial, as it is assumed the student is now familiar with the screens from the tutorial: "Inverter Tutorial on Mixed Signal Simulation w/Verilog"

USING VERILOG TO TEST A 2-INPUT NAND GATE LAYOUT:

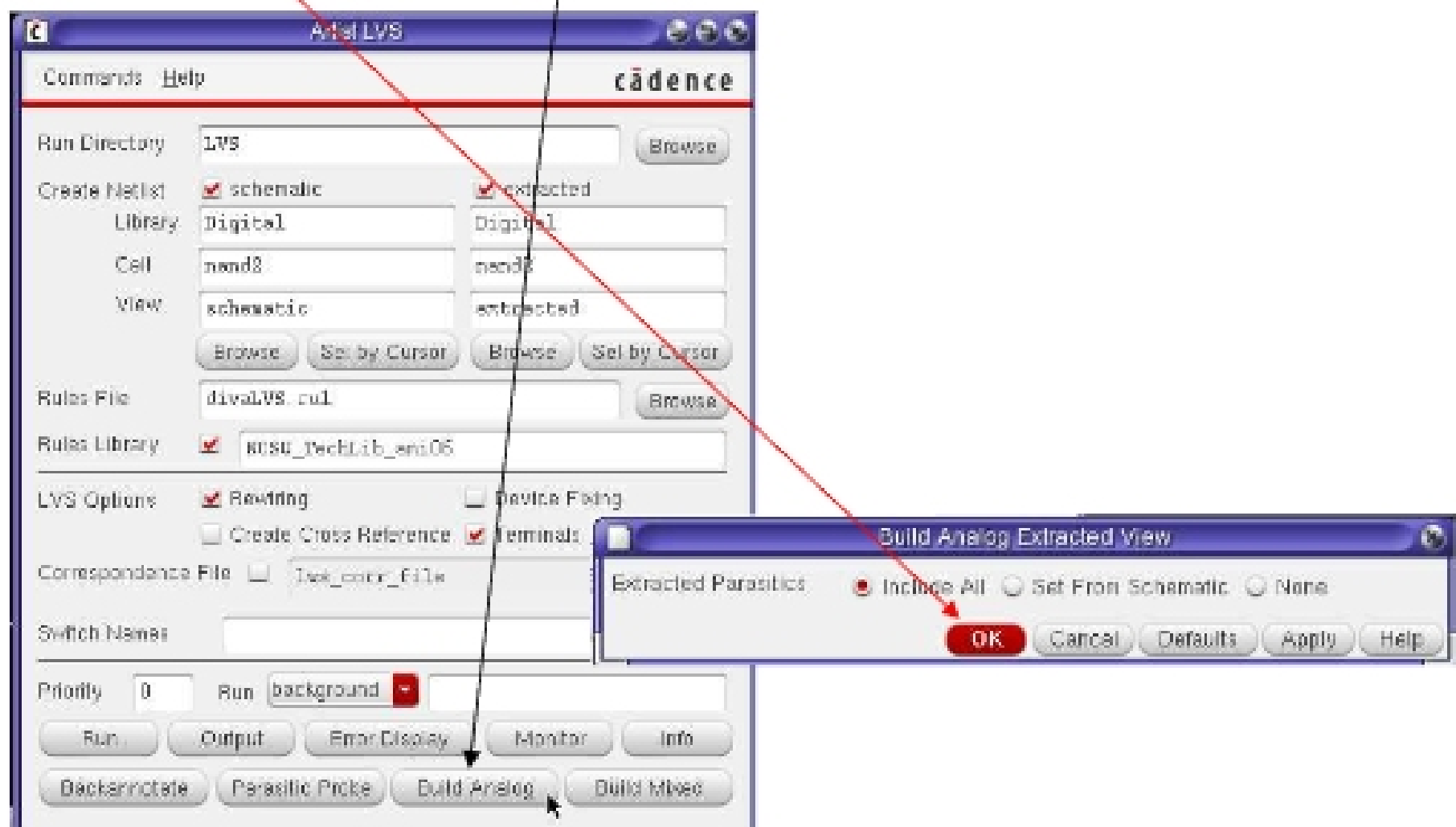
We will now repeat the process, but now for a two-input NAND gate. There are some differences between the work we've done in the last section and what must be done for a two-input NAND:

- The verilog code is slightly more complicated
- The wiring of the test-bench schematic is harder
- We will simulate off the extracted view of the NAND's layout, as opposed to the schematic view.
- We will set the threshold voltage for a 1 and 0 (5V and 0V) in the simulator
- We will add additional verilog code to verify the NAND's output, instead of simply generating the input

CREATING THE ANALOG-EXTRACTED VIEW:

1. Open the extracted view of the 2-input NAND created in HW #1

- Ensure the view was created with parasitic capacitances (if not, re-extract it)
- Bring up the LVS form (Verify->LVS)
- Run the LVS and ensure it passes (view the output log to make certain)
- After successful LVS, click on "Build Analog" button
- Click "OK" on the next form
- Ensure there are no errors in the CIW window, then close the LVS and extracted view



2. Return the Library Manager

- Ensure there is a NAND-2 "analog_extracted" view for the nand2 cell in the Library Manager
- You may open the view if wish; it is identical in appearance to the extracted view
- While this view appears identical to the extracted view, it is different at the netlist level. We will make use of this view later in the tutorial.

CREATING A VERILOG DRIVER FOR A TWO INPUT NAND GATE:

We will now create verilog code to test the two-inputs of the NAND gate

1. Create a new cell in your **Digital Library**, called: `nand2_tb_vdriver`



2. *Edit the verilog code:*

- **Replace** the skeleton verilog code with the following verilog code (copy & paste this code):