

CPSC 614: Graduate Computer Architecture
Intro to Static Pipelining
Prof. Lawrence Rauchwerger

Based on lectures by
Prof. David A. Patterson
UC Berkeley

Review: Dynamic Examples

- **P6 (Pentium Pro, II, III) successful micro-architecture, even with imitator (AMD Athlon)**
 - Translate most 80x86 instructions to micro-operations
 - » Longer pipeline than RISC instructions
 - Dynamically execute micro-operations
- **“Netburst” (Pentium 4, ...) success not clear**
 - Much longer pipeline, higher clock rate in same technology as P6
 - Trace Cache to capture micro-operations, avoid hardware translation
- **Multithreading to increase performance for servers, parallel programs written to use threads**
 - Extra copies of PCs, Registers per thread; e.g., IBM AS/400
- **Simultaneous Multithreading (SMT) exploit underutilized Dynamic Execution HW to get higher throughput at low extra cost?**

Overview

- **Last 3 lectures: binary compatibility and exploiting ILP in hardware: BTB, ROB, Reservation Stations, ...**
- **How far can you go in compiler?**
- **What if you can also change instruction set architecture?**
- **Will see multi billion dollar gamble by two Bay Area firms for the future of computer architecture: HP and Intel to produce IA-64**
 - 7 years in the making?