Rotary Traveling-Wave Oscillator Arrays: A New Clock Technology

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***Abstract*—Rotary traveling-wave oscillators (RTWOs) represent a new transmission-line approach to gigahertz-rate clock generation. Using the inherently stable *LC* characteristics of on-chip VLSI interconnect, the clock distribution network becomes a low-impedance distributed oscillator. The RTWO operates by creating a rotating traveling wave within a closed-loop differential transmission line. Distributed CMOS inverters serve as both transmission-line amplifiers and latches to power the oscillation and ensure rotational lock. Load capacitance is absorbed into the transmission-line constants whereby energy is recirculated giving an adiabatic quality. Unusually for an *LC* oscillator, multiphase (360°) square waves are produced directly. RTWO structures are compact and can be wired together to form rotary oscillator arrays (ROAs) to distribute a phase-locked clock over a large chip. The principle is scalable to very high clock frequencies. Issues related to interconnect and field coupling dominate the design process for RTWOs. Taking precautions to avoid unwanted signal couplings, the rise and fall times of 20 ps, suggested by simulation, may be realized at low power consumption. Experimental results of the 0.25-μm CMOS test chip with 950-MHz and 3.4-GHz rings are presented, indicating 5.5-ps jitter and 34-dB power supply rejection ratio (PSRR). Design errors in the test chip precluded meaningful rise and fall time measurements.**

***Index Terms*—Clocks, MOSFET oscillators, phase-locked oscillators, phased arrays, synchronization, timing circuits, transmission line resonators, traveling-wave amplifiers.**

I. Introduction

CLOCKING at gigahertz rates requires generators with low skew and low jitter to avoid synchronous timing failures. The notion of a "clocking surface" becomes untenable at gigahertz rates [1], frequently mandating that large VLSI chips are subdivided into multiple clock domains and/or utilize skew-tolerant multiphase circuit design techniques [2].

Techniques such as distributed phase-locked loops (PLLs) [3] and delay-locked loops (DLLs) [4] can control systematic skew to within ± 20 ps, but are complex, introduce random skew (i.e., jitter), and have area penalties. H-tree distribution systems, while simple, are difficult to balance and can use upwards of 30% of a chip's total power budget [5]. All these systems are inherently single-phase, induce large amounts of simultaneous switching noise, and can be highly susceptible to this noise.

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Researchers have therefore looked to alternative oscillator mechanisms for better phase stability and lower power consumption. Previous transmission-line systems such as salphasic distribution [6], distributed amplifiers [7], and adiabatic *LC* resonant clocks [8] provide only a sinusoidal or semisinusoidal clock, making fast edge rates difficult to achieve.

This paper introduces the rotary traveling-wave oscillator (RTWO); a differential *LC* transmission-line oscillator which produces gigahertz-rate multiphase (360°) square waves with low jitter. Extension of the RTWO to rotary oscillator arrays (ROAs) offers a scalable architecture with the potential for low-power low-skew clock generation over an arbitrary chip area without resorting to clock domains. Simulations predict rise and fall times of 20 ps on a 0.25-μm process and a maximum frequency limited only by the f_T of the integrated circuit technology used.

Experiments show that although the RTWO operates differentially, careful attention is required to guard against magnetic field couplings between the clock conductors and other structures if the potential performance of these oscillators is to be realized.

II. Concept of the Rotary Clock Oscillator

A. Fundamentals and Structures

The basic ROA architecture is shown in Fig. 1. A representative multigigahertz rotary clock layout has 25 interconnected RTWO rings placed onto a 7×7 array grid. Each ring consists of a differential line driven by shunt-connected antiparallel inverters distributed around the ring. This arrangement produces a single clock edge in each ring which sweeps around the ring at a frequency dependent on the electrical length of the ring. Pulses are synchronized between rings by hard wiring which forces phase lock.

Fig. 2 illustrates the theory behind the individual RTWO. Fig. 2(a) depicts an open loop of differential transmission line (exhibiting *LC* characteristics) connected to a battery through an ideal switch. When the switch is closed, a voltage wave begins to travel counterclockwise around the loop. Fig. 2(b) shows a similar loop, with the voltage source replaced by a cross-connection of the inner and outer conductors to cause a signal inversion. If there were no losses, a wave could travel on this ring indefinitely, providing a full clock cycle every other rotation of the ring (the Möbius effect).

In real applications, multiple antiparallel inverter pairs are added to the line to overcome losses and give rotation lock. Rings are simple closed loops and oscillation occurs spontaneously upon any noise event. Unbiased, startup can occur in

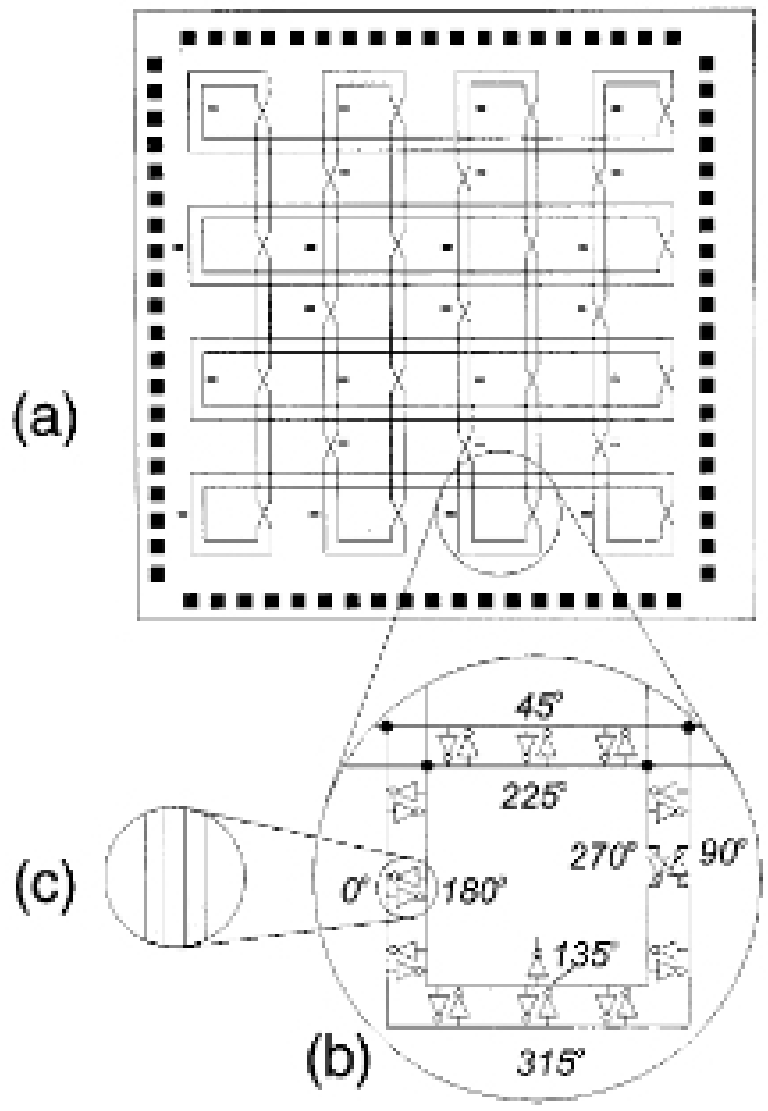

Fig. 1. Basic rotary clock architecture. The = signs denote points with same phase.

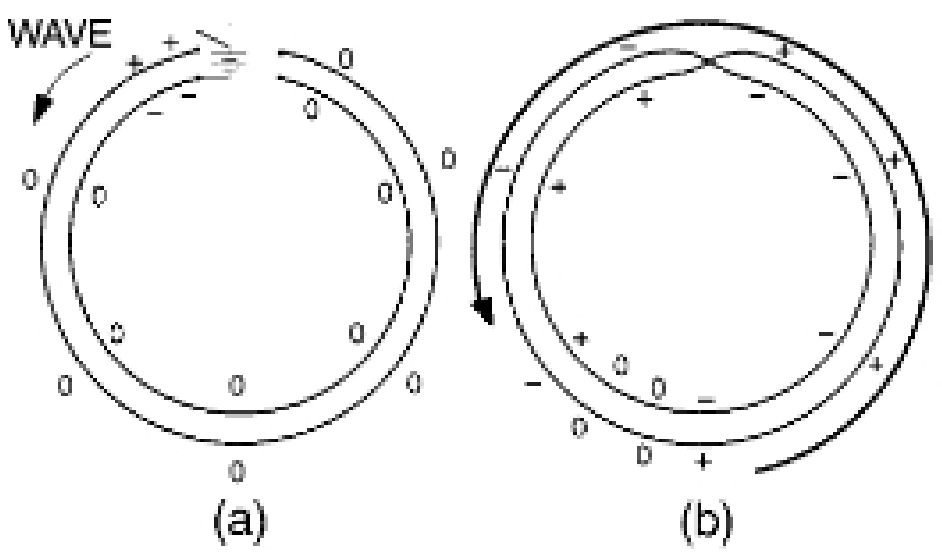

Fig. 2. Idealized theory underlying the RTWO. (a) Open loop of differential conductors to a battery via a switch. (b) Similar loop but with the voltage source replaced by the inner and outer conductors cross-connected.

either rotational sense—usually in the direction of lowest loss. Deterministic rotation biasing mechanisms are possible, e.g., directional coupler technology or gate displacement [9]. Once a wave becomes established, it takes little power to sustain it, because unlike a ring oscillator, the energy that goes into charging and discharging MOS gate capacitance becomes transmission line energy, which is recirculated in the closed electromagnetic path. This offers potential power savings as losses are not related to CV^2f but rather to I^2R dissipation in the conductors where R can be reduced, e.g., by adoption of copper metallization.

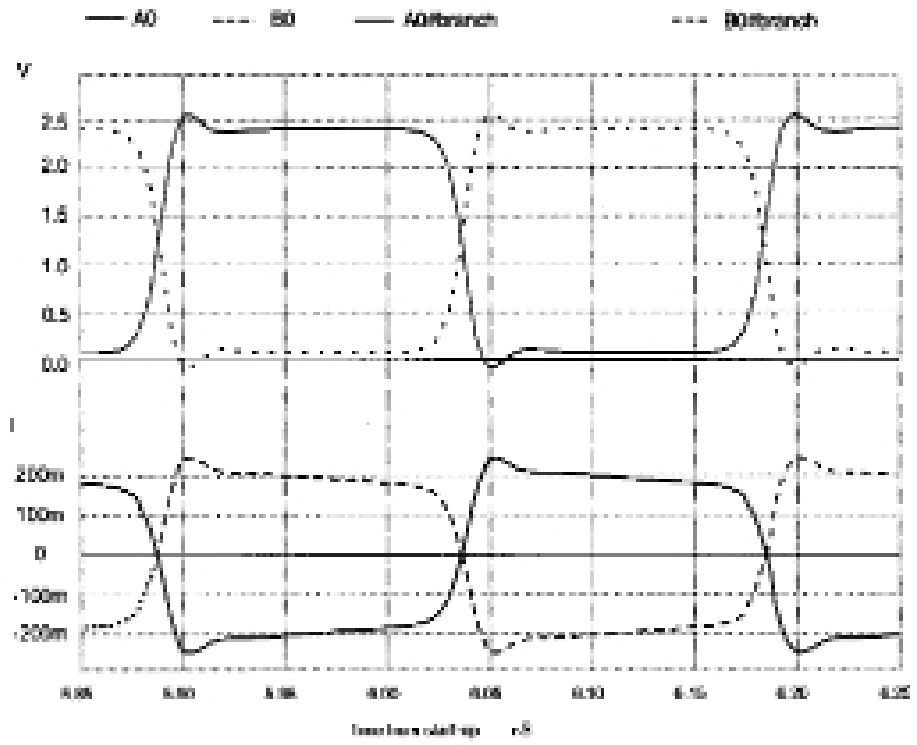

Fig. 3. Waveforms of line voltage and line current for the 3.4-GHz clock simulation example.

B. Waveforms

Fig. 3 shows simulated waveforms of a 3.4-GHz RTWO taken at an arbitrary position on the ring. The design has the following characteristics for reference:

- Conductors: Width = 20 μm
- Pitch = 40 μm
- Ring Length = 3200 μm
- Metallization: 1.75 μm copper
- Loop inductance total = 1.87 nH
- Process: 0.25-μm CMOS
- Nch total width: 2000 μm
- Pch total width: 5000 μm
- Number of inverters: 24 pairs.

Very large distributed transistor widths give substantial capacitive loading to the lines, thus lowering velocity to give a reasonably low clock rate from a compact oscillator structure. In application, up to 75% of this capacitance can come from load capacitance, reducing the size of the drive transistors accordingly.

The upper traces of Fig. 3 show the simulated voltage waveforms on the differential line at points labeled A0, B0. The lower traces show the current in the conductors to be ±200 mA, while the supply current is simulated at 84 mA with ±4.5 mA of ripple. This clearly illustrates that energy is recycled by the basic operation of the RTWO. Just driving the 34 pF of capacitance present would require 275 mA at this frequency (from CVf).

C. Phase Locking

Interconnected rings, as in Fig. 1(a), will run in lockstep, ensuring that the relative phase at all points of an ROA are known. It is possible to use a large array of interconnected rings to distribute a clock signal over a large die area with low clock skew. For example, referring to Fig. 1(a), all the points marked with the equals sign (=) have the same relative phase as that arbitrarily marked as 0°. At any point along the loop, the two signal conductors have waveforms 180° out of phase (two-phase

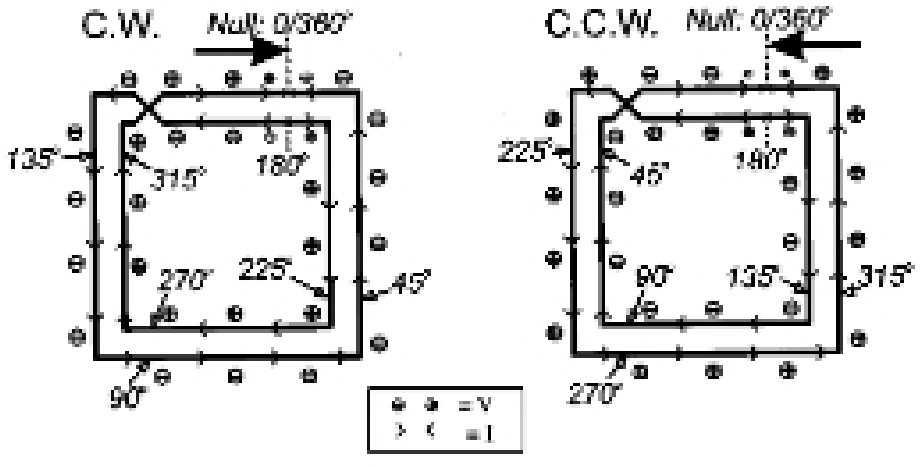

Fig. 4. Voltage, current, and phase relationships versus rotation direction (Poynting's vector).

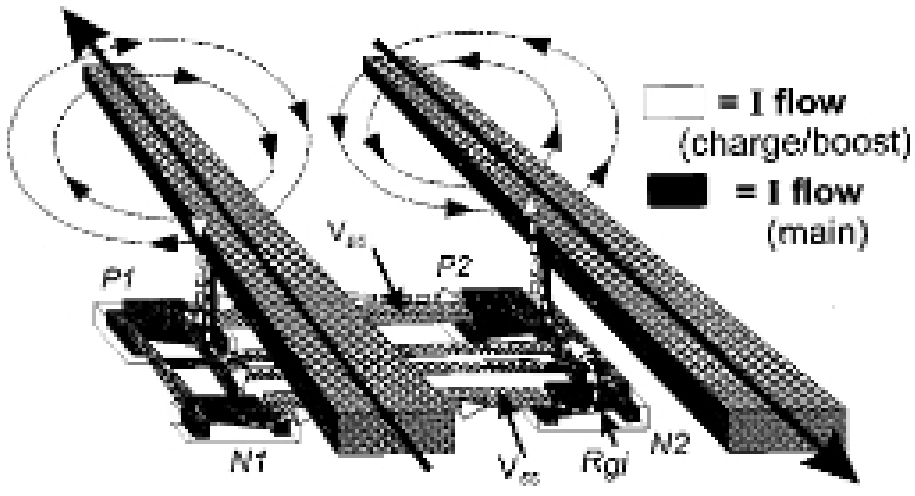

Fig. 5. Three-dimensional view of the structure. The two differential lines are shown, with current flow arrows (main and charge/boost) and encircling H-fields. CMOS transistors are also shown complete with supply voltages (V_{DD} and V_{SS}) and both p- and n-channels.

nonoverlapping clock). A full 360° is measured along the complete closed path of the loop. In principle, an arbitrary number of clock phases can be extracted. Phase advances or retards depend on the direction of rotation, and Fig. 4 shows the current–voltage relationships for clockwise and counterclockwise rotation.

D. Network Rules

Although the square-ring shape is convenient to show diagrammatically, it is only one example of a more general network solution which requires ROAs to conform closely to the following rules.

1) Signal inversion must occur on all (or most) closed paths.
2) Impedance should match at all junctions.
3) Signals should arrive simultaneously at junctions.

From 1) above, any *odd number* of crossovers are allowed on the differential path and regular crossovers forming a braided or "twisted pair" effect can dramatically reduce the unwanted coupling to wires running alongside the differential line.

The differential lines would typically be fabricated on the top metal layer of a CMOS chip where the reverse-scaling trend of VLSI interconnect offers increasingly high performance [10].

E. Fields and Currents

Fig. 5 illustrates a three-dimensional section of the ring structure connected to a pair of CMOS inverters expanded to show the four individual transistors. The main current flow in the differential conductors is shown by solid arrows, the magnetic field surrounding these conductors by dashed loops, and the capacitance charge/signal-boost current flowing through the transistors by dashed lines.

An important feature of differential lines is the existence of a well-defined "go" and "return" path which gives predictable inductance characteristics in contrast to the uncertain return-current path for single-ended clock distribution [11].

Capacitance arises mainly from the transistor gate and depletion capacitance and interconnect capacitance does not dominate.

R_{gi} indicates intrinsic gate resistance, i.e., the ohmic path through which the gate charge flows. The term R_{gi} implies a parasitic gate term, but in reality, most of this resistance is in the series circuit of the channel under the gate electrode. This is shared by the D-S channel, as illustrated by the triangular region (shown with transistors operating in the pinchoff region).

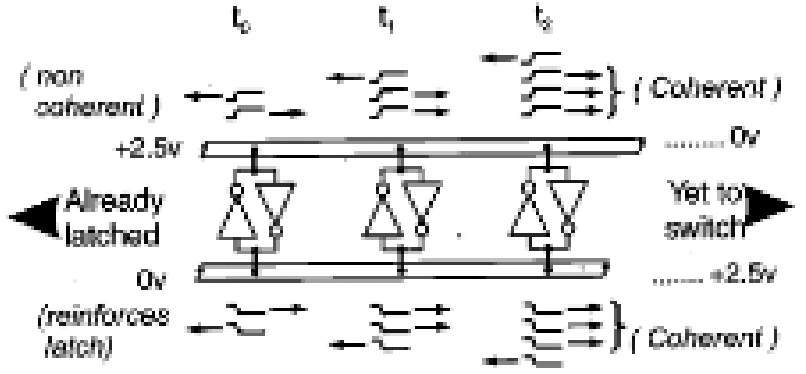

Fig. 6. Expanded view of short sections of the transmission line, including three sets of back-to-back inverters as a wavefront passes.

F. Coherent Amplification, Rotation Locking

Fig. 6 is an expanded view of a short section of transmission line with three sets of back-to-back inverters shown. It is assumed that startup is complete and the rotating wave is sweeping left to right. For this analysis, we view the inverter pairs as discrete latch elements.

Each latch switches in turn as the incident signal, traveling on the low impedance transmission line, overrides the ON resistance of the latch and its previous state. This "clash" of states occurs only at the rotating wavefront and therefore only one region is in this cross-conduction condition at any one time. The transmission-line impedance is of the order of 10 Ω and the differential on-resistance of the inverters is in the 100-Ω–1-kΩ range, depending on how finely they are distributed throughout the structure.

Once switched, each latch contributes for the remainder of the half cycle, adding to the forward-going signal. Coherent buildup of switching events occurs in this forward direction only. An equal amount of energy is launched in the reverse direction, but the latches in that direction cannot be switched further into the state to which they have already switched. The reverse-traveling components simply reduce the amount of drive required from those latches.

Importantly, it is the nonlinear latching action which is responsible for the self-locking of direction (a highly linear amplifier has no such directionality).

To clarify the above statements, Fig. 7 demonstrates how a large CMOS latch responds to an imposed differential signal. The curve trace shows a central differential-amplification region bounded by two absorptive ohmic regions (shaded) corre-