Lecture 18: Output Stages

- **Announcements:**
  - Graded Midterm Exam: will hand back with solutions towards the end of lecture today
  - HW#8 online
  - Lab#3 online today
  - I will be traveling on Thursday, so need to do a make-up lecture
  - Make-Up Lecture: Wednesday, 3/30, 7-8:30 p.m., in 521 Cory (the Hogan room)
  - Again, I will be using software local to my computer to record the lecture
- **Lecture Topics:**
  - Go through Lab#3
  - Output Stages
  - Class A & B
  - Go through Midterm Exam & hand back
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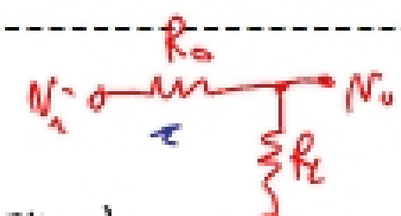
- **Last Time:**



Output Stages

- Class A (Emitter & Source Follower)
- Class B
- Class AB (we'll do this one later)

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + R_o}$$

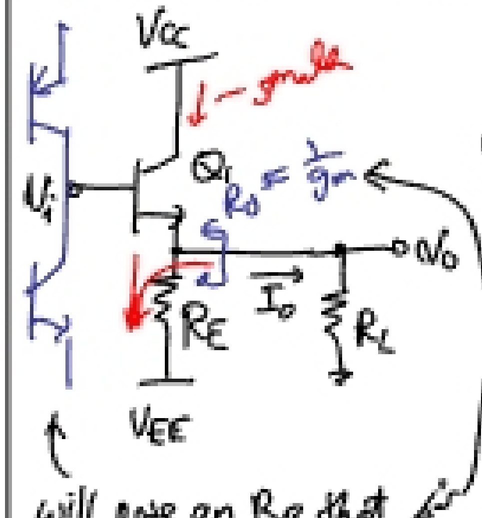
Purpose: Drive loads

1. Deliver power w/ small distortion.
2. Minimize output impedance → so that the amplifier gain is insensitive to the load.

Desirable Attributes:

1. High R_{in}; Low R_{out}.
2. Low quiescent power.
3. Minimal effect on the amplifier freq. response. ← may add freq. poles
4. Should be able to handle large input/output swings. (i.e., v_i may be $> V_T$, invalidating small-signal approximations)

Emitter Follower (Class A)



Two Main Cases:

1. $I_o > 0$: I_o comes from Q_1 → adequate I_o can be supplied so long as Q_1 stays in forward-active
2. $I_o < 0$: (i.e., V_o: (−)) I_o must be sunk to V_{EE} through R_E

$$I_o = \frac{V_o - V_{EE}}{R_E}$$ → gets smaller as $V_o \downarrow$

as $V_o \downarrow$ → $I_o \downarrow$

Problem!

↓ solution

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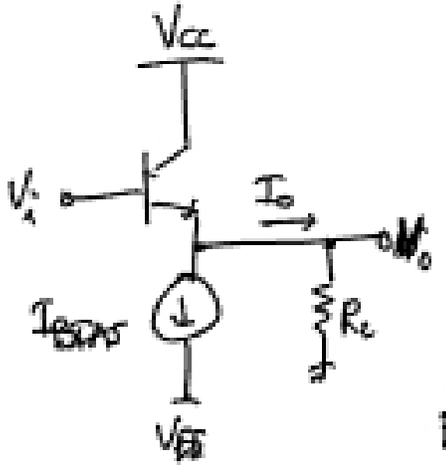
Solution: Replace R_E w/ a current source



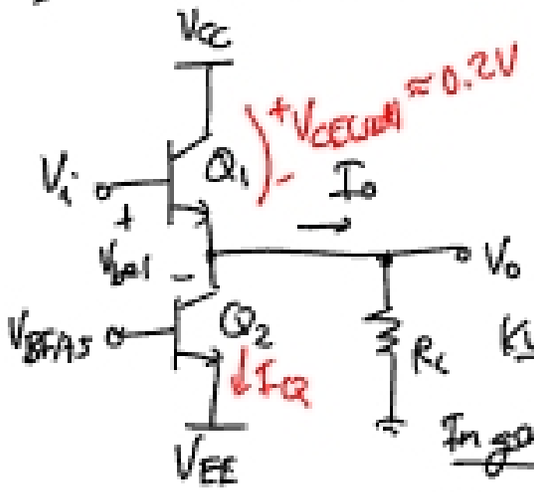
Now, can source I_o thru Q_1 for CMly going V_o.

And can sink $I_o = I_{BIAS}$ (on load)

$\Rightarrow$ I_o does not get smaller as V_o decreases

↳ can maintain drive power! ✓

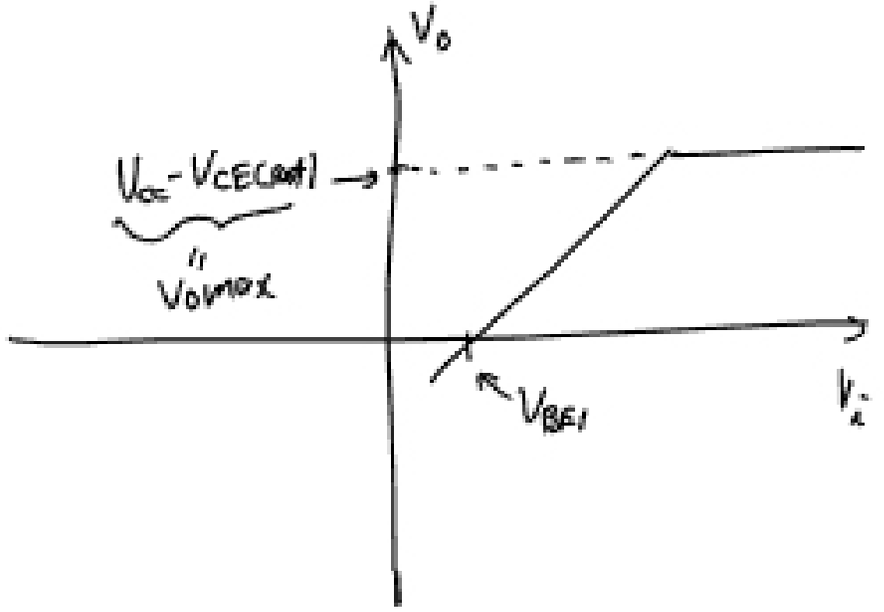
Actual Implementation:



KVL: $V_i = V_o + V_{be1}$

In general:

$V_{be1} \simeq$ const. $\rightarrow V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right)$



Two Cases:

Case ①: R_L large ↗ $I_o < I_Q$

$\Rightarrow$ I_o not Δ'ing much to get a large ΔV_o

For V_i large and (+): Q_1 must source $I_o + I_Q$ to make V_o ↑

↳ at some pt., Q_1 will saturate as V_o ↑

↳ $V_{omax} = V_{cc} - V_{CE(sat)}$

↳ and V_i: $V_{cc} - V_{CE(sat)} + V_{BE1}$

not always possible if input signal is limited by Vcc supply rail

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- Now, distribute graded midterm exams and go through grading and what everything means

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