Veriolog Overview

CS/EE 3710
Fall 2010

Hardware Description Languages

- HDL
  - Designed to be an alternative to schematics for describing hardware systems
- Two main survivors
  - VHDL
    - Commissioned by DOD
    - Based on ADA syntax
  - Verilog
    - Designed by a company for their own use
    - Based on C syntax

Verilog Origins

- Developed as a proprietary HDL by Gateway Design Automation in 1984
  - Acquired by Cadence in 1989
  - Made an open standard in 1990
  - Made an IEEE standard in 1995
  - IEEE standard Revised in 2001

Verilog

- You can think of it as a programming langauge
  - BUT, that can get you into trouble!
- Better to think of is as a way to describe hardware
  - Begin the design process on paper
  - Plan the hardware you want
  - Use Verilog to describe that hardware

Quick Review

```
Module name (args…);
  begin
    parameter ...; // define parameters
    input …;   // define inputs
    output …; // define outputs
    wire … ;   // internal wires
    reg …;     // internal regs, possibly output
   // the parts of the module body are
   // executed concurrently
     <continuous assignments>
     <always blocks>
endmodule
```

Quick Review (2001 syntax)

```
Module name (parameters, inputs, outputs);
  begin
    wire … ;   // internal wires
    reg …;     // internal regs
   // the parts of the module body are
   // executed concurrently
     <continuous assignments>
     <always blocks>
endmodule
```