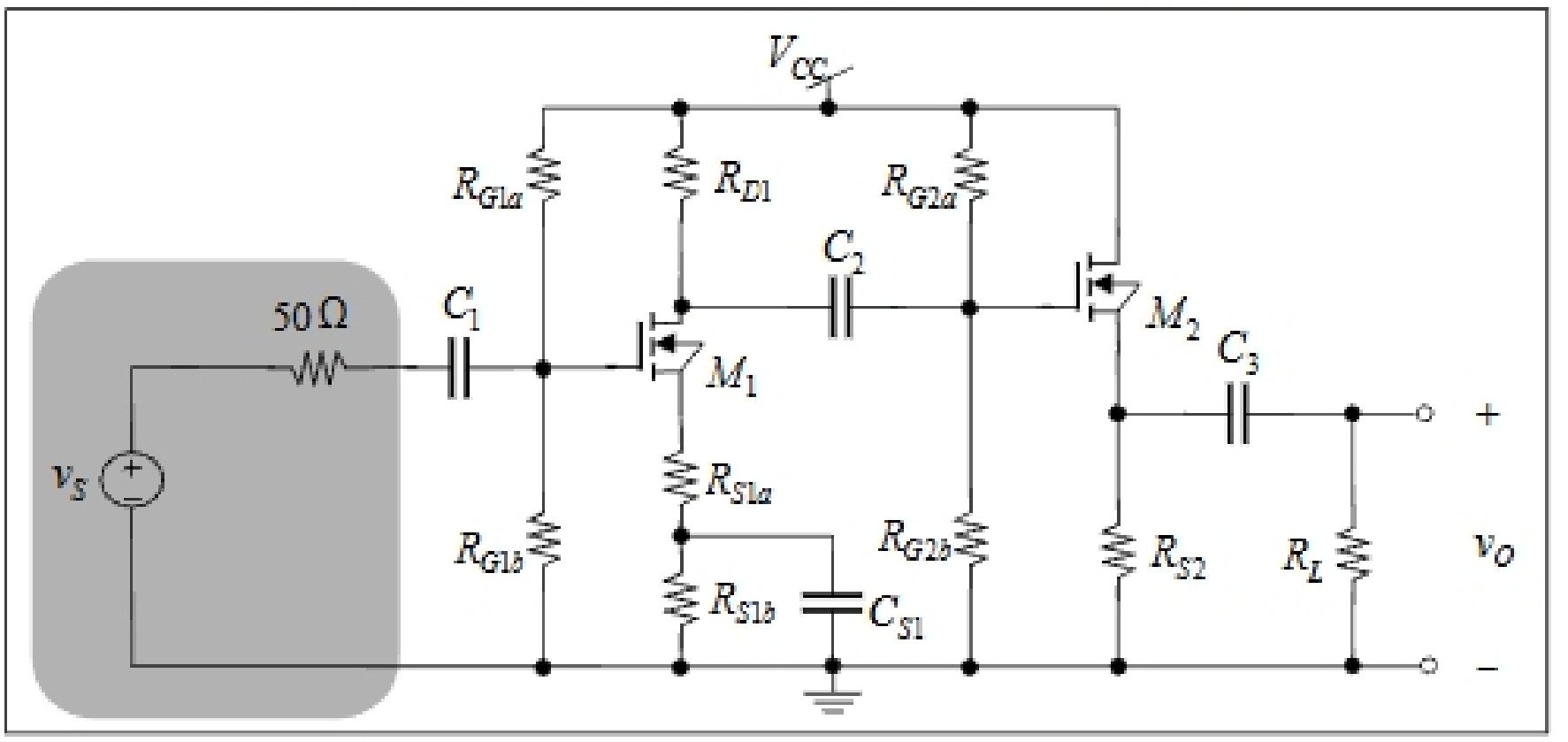
**EGRE224** **Spring '01**

# DESIGN PROJECT

## Two-stage MOS Amplifier with Specified Performance

- Purpose: The purpose of the EGRE 224 Design Project is for you to apply the procedures commonly used to analyze fundamental electronic circuits by successfully designing, building and testing an electronic circuit of sufficient complexity. This design project is to be done in groups of two (2) **ONLY**!
- Specifics: You will design, simulate, build and test an amplifier using two NMOS (VN2222LL) enhancement mode field effect transistors. Your amplifier must meet the following specifications:
  A) Topology: You must adhere to the circuit topology shown below:




| | | |
|---|---|---|
| B) | Voltage Gain: | 27 dB ±1dB @ f=10kHz (midband) |
| C) | Load: | 100Ω ± 5%, ¼-Watt resistive load |
| D) | Lower cut-off frequency: | -3dB ± ½dB @ f≤200Hz |
| E) | Upper cut-off frequency: | -3dB @ f≥10MHz |
| F) | Source: | 100mVp-p sinusoid with a 50Ω internal resistance |
| G) | Distortion: | NO visible output distortion for $v_S$ < 100mVp-p |
| H) | Power Supply: | +15 VDC |
| I) | Efficiency: | > 15% |
| J) | Components: | $C_1$, $C_2$, $C_3$ < 100∝F, $R_{S1a} \geq 50\Omega$, standard values for resistors and capacitors, all resistors to be ¼-Watt unless you specify otherwise |

- Submissions: You must submit the following documents for your project:
  1. Intermediate Project Review (10 points). The IPR is an oral and written report on your design in the instructor's office. You will be submitting a written report but you should also show your instructor the work done in your lab notebook in arriving at the results you present. Your written report covers the design theory listed below and consists of hand calculations and/or MathCad documents showing your initial design calculations. The use of software like MathCad is very helpful since it allows you to make design changes and easily recalculate your results.
     - Design Theory
       - All quiescent currents and voltages
       - Standard 5% resistor values and capacitor values
       - SPICE Model parameters used
       - Small-signal parameters and midband gain
       - Input and output resistance of both stages

     Prepare your IPR well! You'll have only ten minutes to tell your instructor what your plan is for your design. If you're not prepared, or don't understand what's going on, you'll lose most of the points alloted to this portion of the design project.
  2. Design Demonstration (40 points). Your circuit will be demonstrated to your instructor in the laboratory to prove that it meets all of the design criteria. Your entire design values and final simulation printouts done in ACCUSIM (these should be in your final report) will be available for comparison to actual measurements. You should do a transient simulation at midband frequencies to see if there is any clipping of the signal. You should also do an ac (Bode Plot) simulation to find the amplifier's frequency response. The data collected in lab should also included in your final report. Measurements will be taken on an HP DMM, the HP4194A gain-phase analyzer and an oscilloscope. As a minimum, have your simulations of:
     - All DC operating conditions.
     - Transient output simulation at an input frequency of 10kHz
     - Gain (dB) plot versus frequency with labels for midband gain and cut-off frequencies.
     - Plot of output voltage waveform vo(t) and input voltage waveform vs(t).
  3. Final Written Report (50 points) The final written report will reflect your theory, test procedures, equipment used, laboratory measurements, and the comparison of experimental results with theoretical values. A table of contents must be included. Focus your efforts on error analysis and a complete discussion of your design process. You should be keeping records of your project as the work progresses. 50% of the grade on the final report will be allocated to your design process. Simply having a working amplifier that meets the specifications is not enough. You must show how you performed the trade-off analysis in the design of each stage in order to calculate the DC bias point, per-stage gain, and the required component values.

- Schedule: To ensure that the project is done on time and in a satisfactory manner the following timetable of events must be adhered to:

| Date | Time | Submissions |
|---|---|---|
| Week of April 9th-13th | Before 5:00 PM on the day of your lab | Intermediate Oral/Written Project Review |
| Week of April 23rd-27th | Before the end of your lab | Design Demonstration |
| Tuesday, May 1st | Before 5:00 PM | Written Report |