

LAr high speed optical link studies: the status report on the LOC ASIC

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Datao Gong, Andy Liu, Annie Xiang and Jingbo Ye
Department of physics, SMU





The LOC ASIC, an introduction

- The LOC (link-on-chip) was proposed as a serializer ASIC for the ATLAS LAr readout upgrade, under the US-ATLAS upgrade program.
- The initial idea was to integrate “everything” into one chip, including the optical interface. Fiber would be coupled directly to the chip to spare high speed copper traces on the PCB.
- The project started with the SOS technology evaluation in 2006.
- A first prototype, LOC1 was designed with collaborative effort between the EE and physics departments at SMU 2007. This prototype provided valuable information on key components, especially the PLL and the serializer structure, for the LOC2 design.
- The second prototype, LOC2 is being designed as a 5 Gbps serializer ASIC. This design takes advantage of the CERN common project, the Versatile Link, and uses it as its optical interface. The submission is April 2009.
- The whole project benefits tremendously from the CERN GOL ASIC design. We would like to express our gratefulness to many people in the CERN microelectronics group, especially to Paulo Moreira for his very kind help in the LOC project.

The SOS technology

- A 0.25 micron Silicon on Sapphire commercial CMOS technology has been chosen for the LOC ASIC development.
- A dedicated test chip with transistors, ring oscillators and shift registers has been designed and fabricated for irradiation tests.
- Some results from the irradiation tests have been published at RADECS 2007.
- The TID test results on transistors are summarized here. The substrate is grounded.
 - Almost no leakage current change;
 - A small threshold voltage change happens at the very beginning of the irradiation and then remains unchanged with the increase of total dose.
- The technology evaluation continues with more detailed studies, supported by the ADR (US DOE) program.

