

Last Name (Print): _____

First Name (Print): _____

ID number (Last 4 digits): _____

Section: _____

Submission deadlines:

- Upload the Ultiboard file for Problem 21 to the Angel drop box by midnight on Tuesday February 25.
- Update your e-Portfolio for Problem 22 by midnight on Tuesday February 25.
- Turn in the written solutions for problems 23 and 24 by 4:00 pm on Tuesday February 25 in the homework slot outside 121 EE East.

Problem	Weight	Score
21	35	
22	20	
23	20	
24	25	
Total	100	

Problem 21: (35 points)

Generate a printed circuit board layout for just the clock circuit of the robot navigation FSM using Ultiboard. To receive credit, adhere to the following guidelines.

- Transfer the schematic in Multisim file `ps6_p21_clk_schematic.ms12` to Ultiboard.
- Use a two-layer circuit board that measures 1.0 inches high by 1.0 inches wide.
- Use a ground plane on the bottom layer and run signal traces on the top layer.
- All components should mount on the top side of the board.
- Use the footprints specified in the Multisim file.
- Position the power input and clock output headers on the upper and lower right side of the board, respectively.
- Position U1 so that pin 1 is on the upper left hand side.
- Use a silk screen layer to label components.
- To receive credit, upload the Ultiboard file to the Angel drop box by midnight on Tuesday February 25 using the following syntax

`xyz_ps6_p21.cwprj`

where `xyz` represents the last four digits of your Penn State ID number.

The grader will award credit on the following basis:

1. (5 points) The board measures 1.0 inches high by 1.0 inches wide.
2. (5 points) The bottom layer is a ground plane and the signal traces appear on the top layer.
3. (5 points) All components mount on the top side of the board and use the footprints specified in the Multisim file.
4. (5 points) The headers and IC are positioned as specified above.
5. (5 points) Each component has a silk-screen label, and the silk-screen title **Clock Generator** is centered along the top of the board.
6. (5 points) The layout must adhere to the guidelines specified in Lecture 5, in particular, slides 30 through 32.
7. (5 points) The layout passes the design rule checks using the DRC tool.

Problem 22: (20 points)

Update and augment your e-Portfolio.

1. This exercise requires you to reflect on what skills you have acquired or demonstrated in EE 200. Under the **GOALS and SKILLS** section, enumerate several skills that you have learned in EE 200 using a list of short bullets, for example,
 - Dataflow programming using LabVIEW and HDL.
2. Under the **WORKS IN PROGRESS** section, include an image and brief description of either the discrete-logic or PLD realization of the finite state machine for navigating the EE 200 mouse.

Problem 23: (20 points)

Figure 1 shows the schematic capture of the parity detector designed in Laboratory #5, while Figure 2 shows a layout using a single copper layer on top of the printed circuit board.

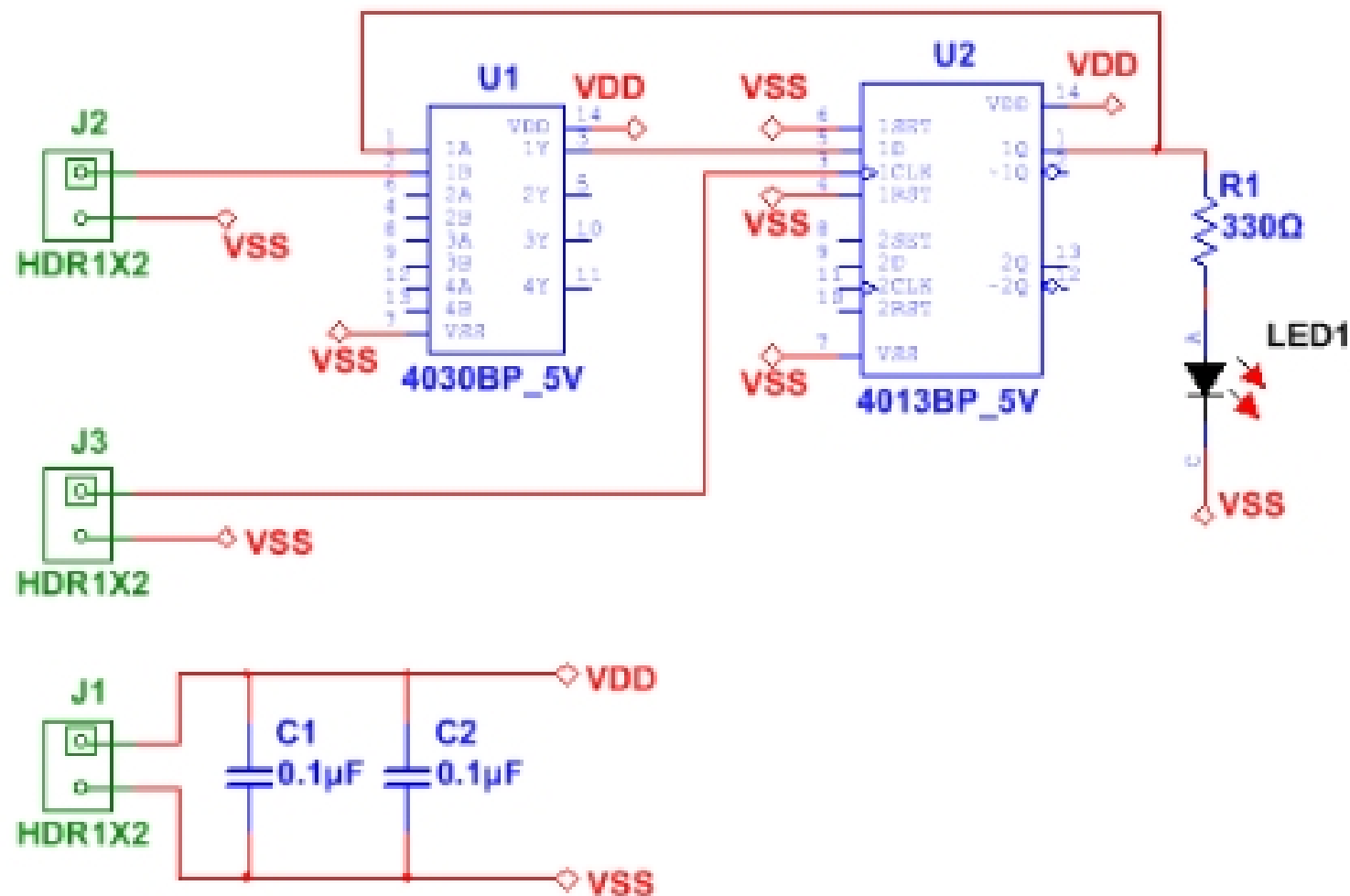


Figure 1: Schematic capture.

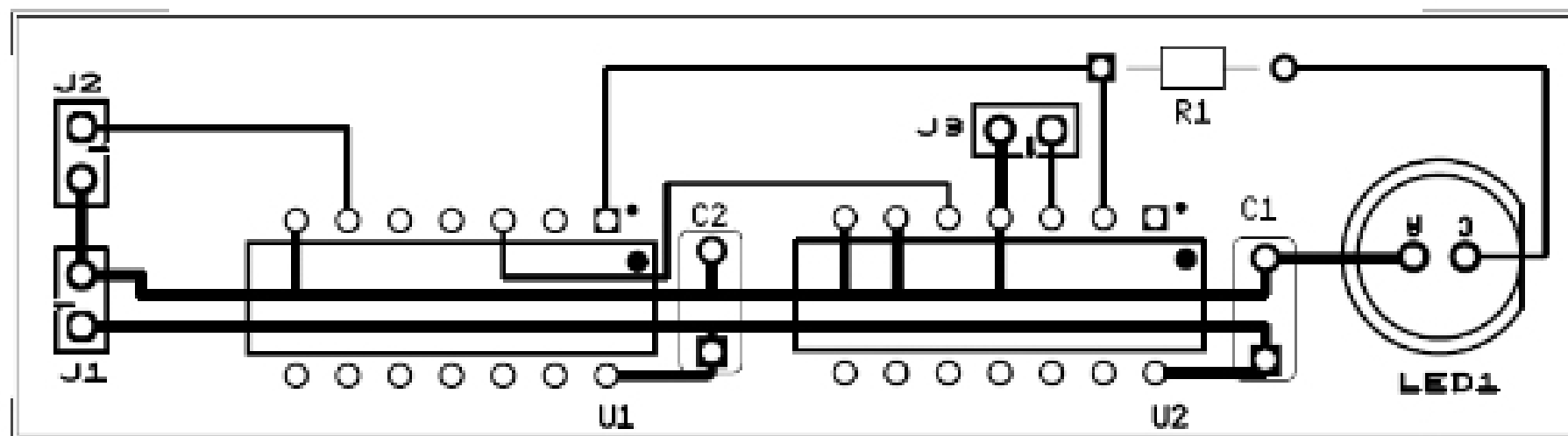


Figure 2: Printed circuit board layout.

- (10 points) Is the printed circuit board layout consistent with the circuit diagram in Figure 2? If not, state the differences.
- (10 points) Regardless of whether or not the circuit layout is consistent with the circuit diagram, critique the layout in Figure 2 with respect to trace routing. What changes would you suggest? Assign each of your suggestions a number, and attach a copy Figure 2 with your your solutions that contains a circle around each affected region and label the circles with the corresponding suggestion number.