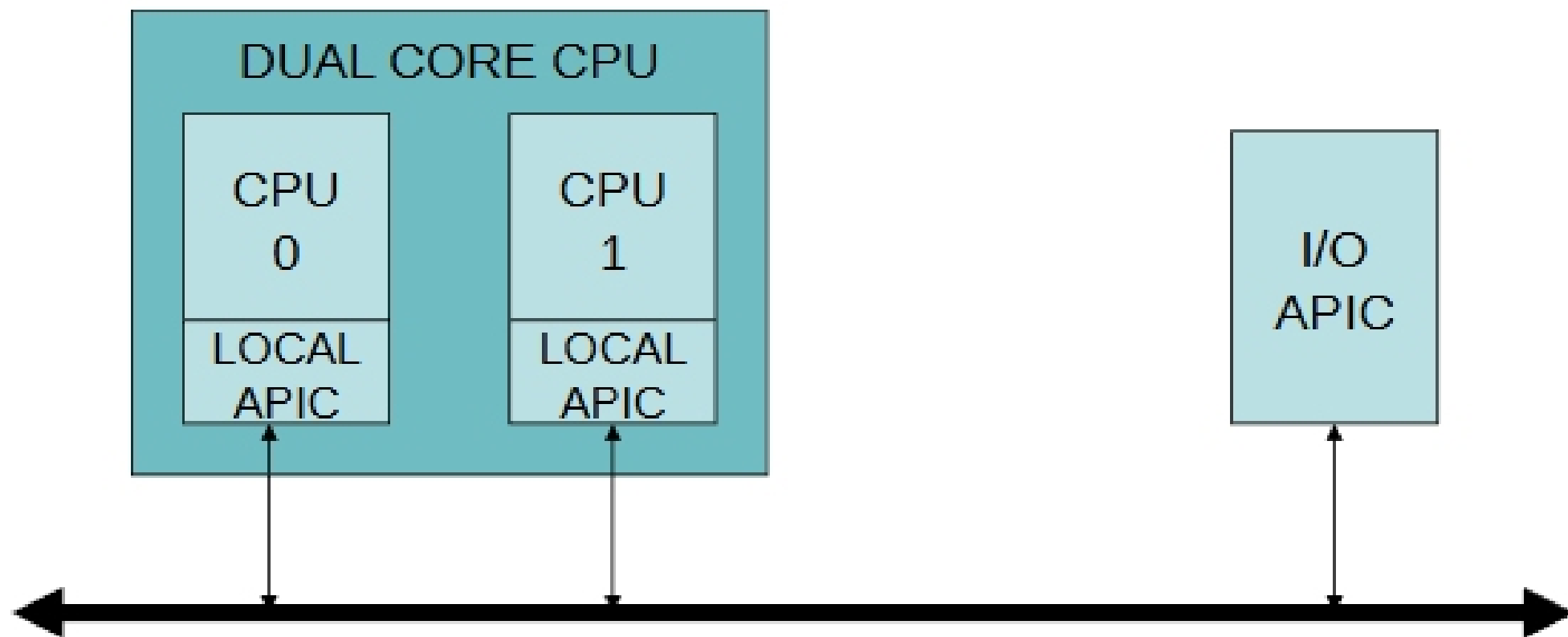


Advanced Programmable Interrupt Controllers

Multiprocessor-systems require enhanced circuitry for signaling of external interrupt-requests

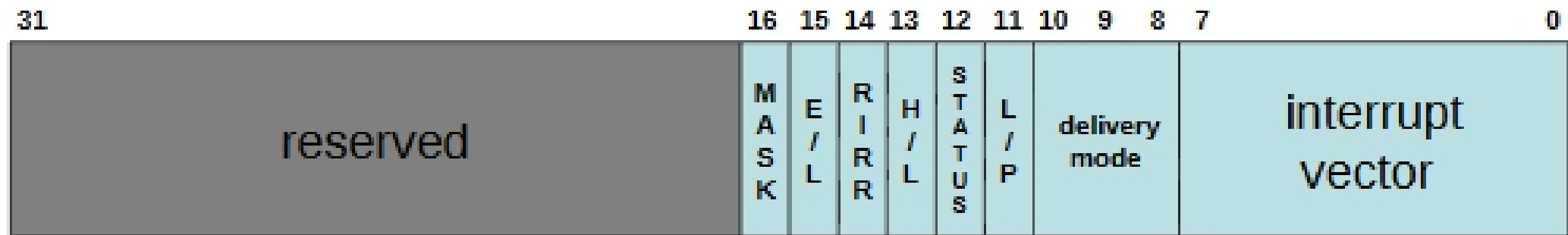
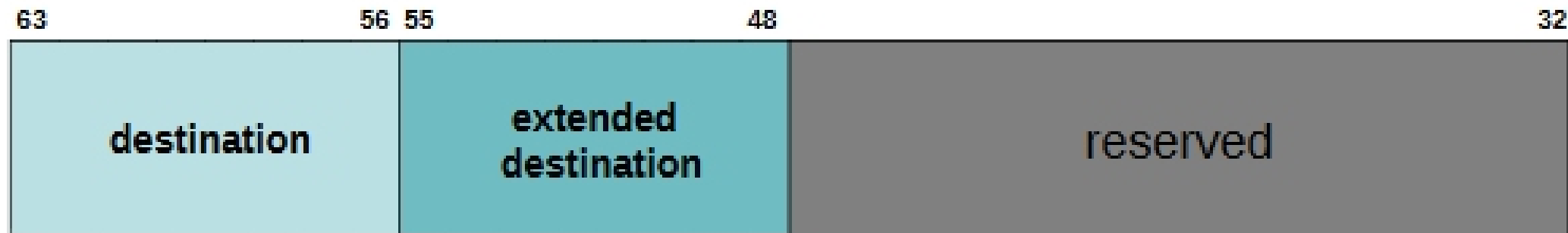
Multiple Logical Processors



Advanced Programmable Interrupt Controller is needed to perform 'routing' of I/O requests from peripherals to CPUs

(The legacy PICs are masked when the APICs are enabled)

Redirection Table Entry



Trigger-Mode (1=Edge-triggered, 0=Level-triggered)

Remote IRR (for Level-Triggered only)
 0 = Reset when EOI received from Local-APIC
 1 = Set when Local-APICs accept Level-Interrupt sent by IO-APIC

Interrupt Input-pin Polarity (1=Active-High, 0=Active-Low)

Delivery-Status (1=Pending, 0=Idle)

000 = Fixed
 001 = Lowest Priority
 010 = SMI
 011 = (reserved)
 100 = NMI
 101 = INIT
 110 = (reserved)
 111 = ExtINT

Destination-Mode (1=Logical, 0=Physical)