Report Guidelines

Your project report should include the following sections:

- Discussion of your topology choice: explain why you chose a certain topology and compare your topology with possible alternatives.
- Discussion of your bandwidth maximization strategy: explain how you chose all the W's, L's, and currents; show your calculations for important poles and zeros.
- Discussion of your strategy to address variation of the supply voltage V_{DD}.
- A schematic of your circuit, annotated with all the node voltages. (for both $V_{DD\text{-}min}$ and $V_{DD\text{-}max}$ on same schematic)
- Provide a table with W, L, and the simulated value of V_{dsat} and I_{ds} for every transistor. For I_{ds}, include the simulated values for V_{DD}=$V_{DD\text{-}min}$ and V_{DD}=$V_{DD\text{-}max}$.)
- Include simulated frequency characteristics curves of small-signal differential and common mode voltage gain (dB) of your amplifier.
- List 3dB-bandwidth, maximum in-band common mode gain, and the worst case total power consumption of your design and compare your calculations and the results from the test benches.
- Comments and conclusion.

Note:
Assume that the power supplied by the 0.6V supply (connected to R_L) is generated by V_{DD}. (therefore the effective total current, I_{DDT}, is equal to $(V_{DD}*I_{DD} - 0.6V*I_L)/V_{DD}$, where I_L is the current delivered to the load by the amplifier.

DO NOT INCLUDE SPICE NETLIST IN THE PROJECT REPORT.

Circuit submission guidelines

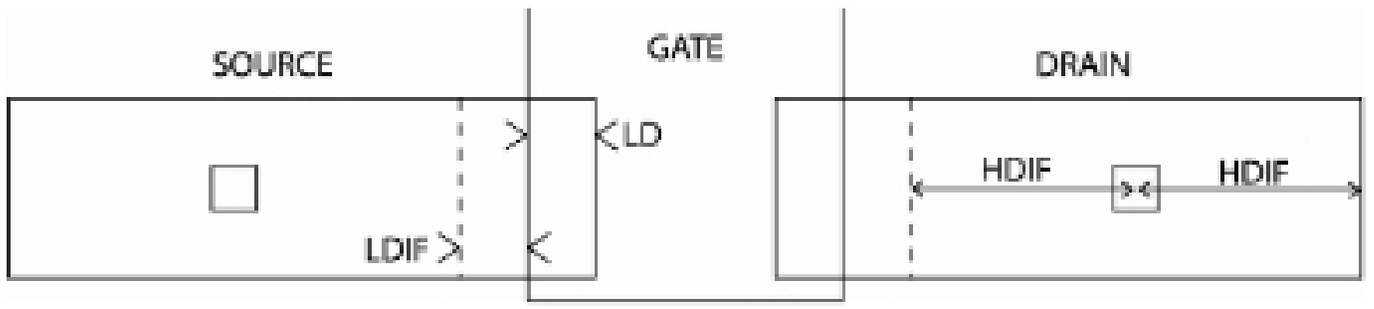
Send an email to ee140@cory.eecs.berkeley.edu with your name in the subject and your circuit in the body of the email. Make sure to send the email in plain text, not in html.
The body of the email should be the same as the file used to run the test bench:

```
.param VIC = < your midpoint of the common mode input range >
.subckt amplifier inp inn out vdd vss
< your circuit >
.ends
```

The subcircuit should be named 'amplifier' and the order of the input nodes should be: positive input node, negative input node, output node, positive supply, negative supply. You can change the names of the nodes.

Transistor Capacitance Parameters

LEVEL=2, ACM=3, GEO=0



AD area of drain $AD = AS = 2 \cdot HDIF \cdot W$
AS area of source

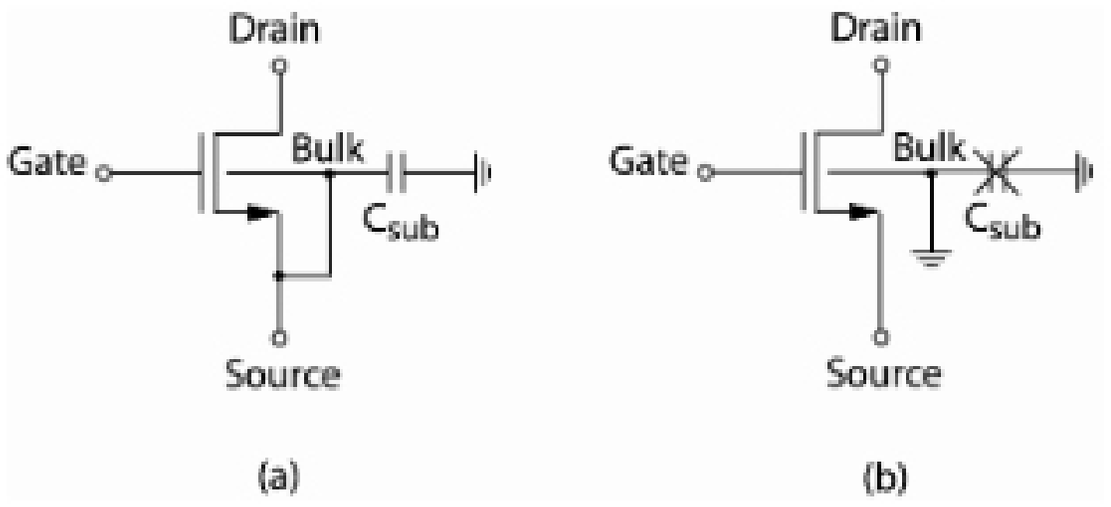
PD, PS periphery of drain (and source). NOT including the gate width since the CJGATE model parameter separately models the drain and source periphery capacitances along the gate edge.

$PD = PS = 4 \cdot HDIF + W$

*C0BD = C0BS = CJ*AD*
*C0BD_SW = C0BS_SW = CJSW*PD + CJGATE*W*

LD lateral diffusion into channel from source and drain diffusion.
If CGD0 (or CGS0) is not set, then the gate-drain (or gate-source) overlap capacitance (per meter channel width) is calculated from LD and TOX.
(you can assume fringing field factor is 0, i.e. no fringing)

C_{SUB} bulk to substrate capacitance.



For this project, we recommend you to connect bulk terminal of all NMOS and PMOS transistors to GROUND and VDD respectively. (Fig. b)

(You need to take into account C_{SUB} in your analysis if bulk terminal of a transistor is not AC grounded (for each individual transistor add its own C_{SUB}, Fig. a). You can assume that $C_{SUB}=C_{SUB0}= CJ*A_{Bulk}$. Where A_{Bulk} (the well area) can be calculated as: $A_{Bulk} = (W+6um)*(L+10um)$. C_{SUB} will be added to the transistor model sub-circuits when we evaluate your design. DO NOT use any capacitor in your netlist.)