

## Optical Receiver Design Project

November 18, 2005

Due: December 6, 2005 on the MIT course website (no later than 12:55PM)  
*(late project reports not accepted)*

### 1. Overview

The explosive growth in data communications has stimulated the development of optical systems for high channel capacity (typically 4-16 channels) and high bandwidth. In a fiber optic system, a transmitter encodes the data in the form of laser pulses that are transmitted over a long optical fiber. At the other end, a receiver detects the attenuated optical signal and amplifies it to digital levels.

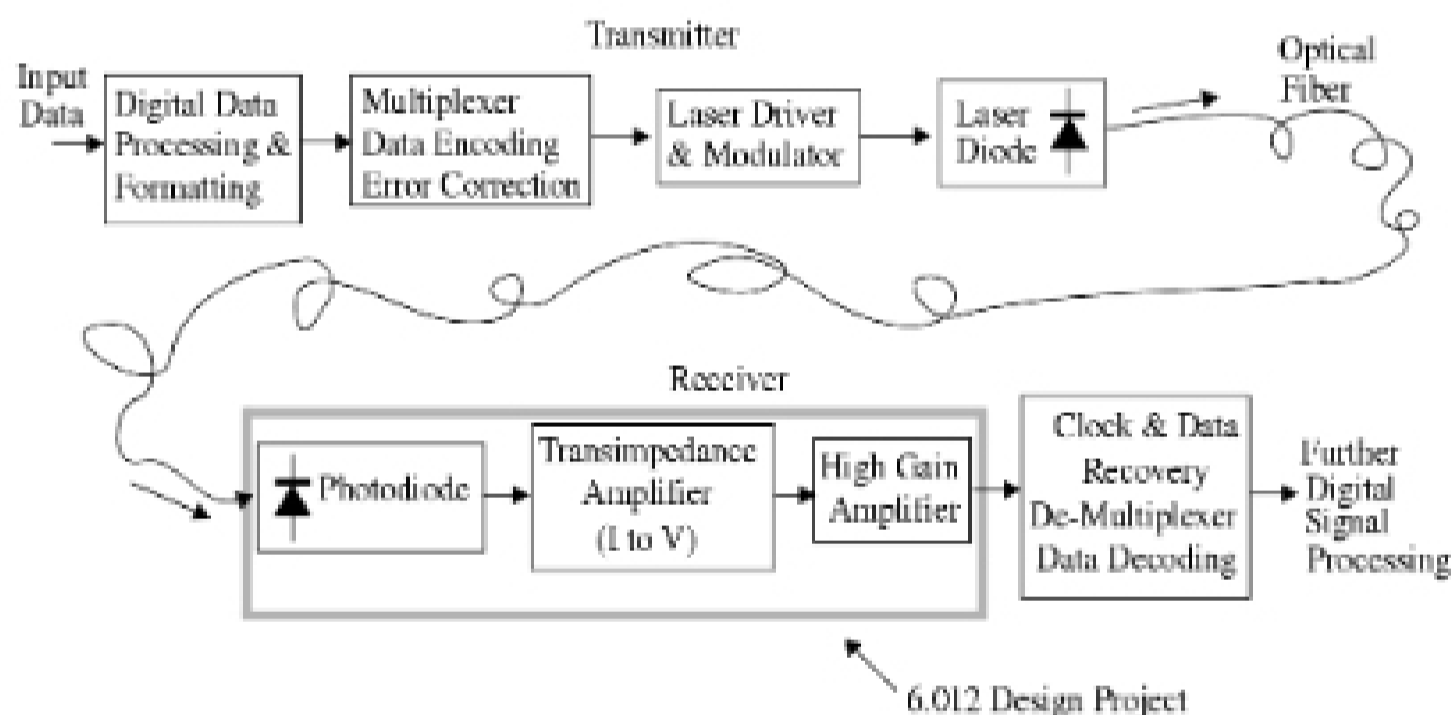


Figure 1: Block diagram of an optical transmitter and receiver.

A block diagram of an optical transmitter and receiver is shown in Figure 1. On the transmitter path, the data is multiplexed, encoded, and error correction bits are added. A laser driver and modulator drive the laser diode, which transmits an optical signal over the fiber. After some loss in the fiber, the optical signal is detected at the receiver end by the photodiode. A transimpedance amplifier converts the small photodiode current into a voltage, which is then amplified to digital levels for subsequent digital signal processing. The transimpedance amplifier is also called a transresistance amplifier in 6.012; for cultural reasons, we will stick with the transimpedance amplifier terminology.

Integration of all of the functions on either side of Figure 1 onto a single CMOS chip would save costs, but the implementation has eluded system designers in part due to the complexity of realizing high-performance receiver circuits in CMOS. The goal of this design project is to design a fast, high gain, low noise, and low power optical receiver in an inexpensive CMOS process.

## 2. Design problem statement

Figure 2 shows the schematic of the optical receiver. It consists of three CMOS stages: a transimpedance amplifier, a saturating or limiting amplifier, and an output driver. We describe these three stages next.

Light creates electron-hole pairs that produce a current  $I_{light}$  in the reverse-biased photodiode. The diode can be modelled as a current source of value  $I_{light}$  which flows in the reverse bias direction of the diode. Although the laser diode produces a large square wave pulse at the other end of the fiber, dispersion and loss make the diode current  $I_{light}$  appear sinusoidal. This current is only guaranteed to have a peak value of about  $10 \mu\text{A}$ . Depending on the system, loss in the fiber could be lower and the peak diode current could be larger. However, to ensure proper operation for all systems, the worst-case (i.e. minimum) current must be used for the design. The receiver should operate at speeds up to 1 MHz.

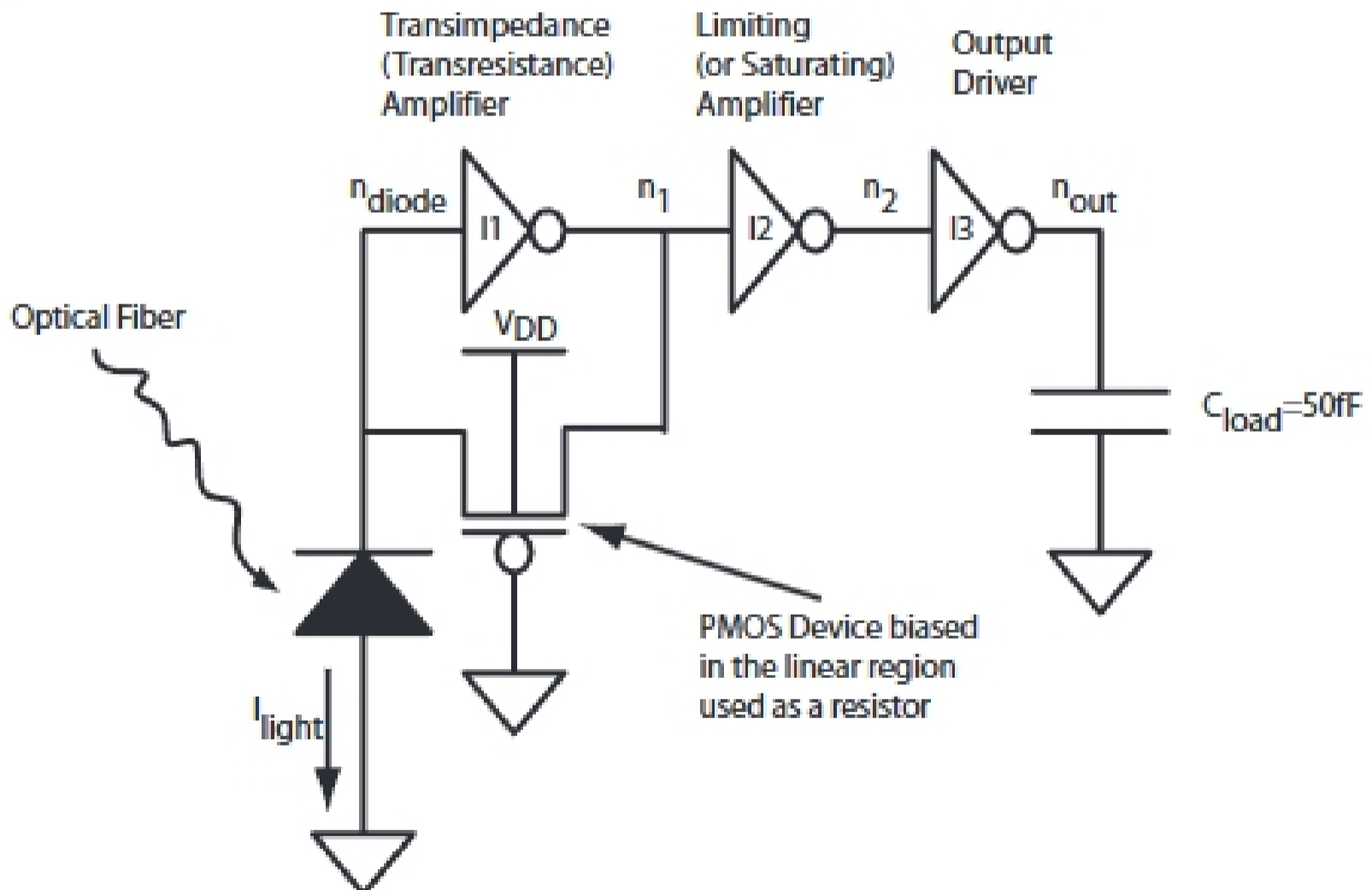


Figure 2: Schematic of optical receiver.

The first-stage CMOS inverter I1 and feedback resistor constitute a transimpedance amplifier that converts the photodiode current into a voltage  $V_1$  at node  $n_1$ . A feedback resistor sets the gain of

the stage, which must be large to reduce the effects of noise in later stages.

To set a reasonable design point you might first want to start by using a simple linear resistor and determine what value you could use to meet your design goals. Unfortunately, though linear resistors can be realized in silicon technology by using undoped poly for large resistor values, this approach consumes a lot of area. With the knowledge of device physics that you have acquired in 6.012, in order to minimize the cost you have decided to realize this resistor using a PMOS biased in the linear region. An additional concern in this amplifier is that the gain needs to be as constant as possible over the expected range of  $I_{light}$  values. This means that the resistor value should be as constant as possible over the range of voltages at its terminals, or, in other words, as linear as possible. Power must be minimized in this design, so no extra bias circuitry can be afforded. The PMOS device is to be connected as shown in Fig. 2 with the gate of the PMOS connected to GND and the bulk connected to  $V_{DD}$ . The design decision that you need to make is to size the PMOS appropriately to achieve the desired value of the resistor.

The closed-loop small-signal gain  $\frac{V_1}{I_{light}}$  of this first transimpedance amplifier needs to be as constant as possible over the range of  $I_{light}$  values shown in Figure 3. You will need to derive an expression for this closed-loop gain  $\frac{V_1}{I_{light}}$ , where  $V_1$  is the voltage at node  $n_1$ . Notice that since  $I_{light}$  is small,  $V_{diodc}$  (the voltage at node  $n_{diodc}$ ) and  $V_1$  will stay close to the midpoint of inverter I1, and I1 will be held in the high-gain region. Thus the transistors in inverter I1 will stay in the saturation region, and the small signal model can be used over the full range of input current. For the  $I_{light}$  shown in Figure 3,  $V_1$  should have a peak-to-peak amplitude of at least  $0.1 V_{pp}$  (peak-to-peak voltage), as indicated in Figure 3. For noise immunity,  $V_1$  should be near the middle of the total voltage range. Therefore, the minimum of  $V_1$  should be at 2.5 V, as indicated in Figure 3. To ensure that the photodiode stays in reverse bias, and in an attempt to keep the depletion region width constant, the reverse biased diode voltage  $V_{diodc}$  should vary by no more than 10 mV peak-to-peak ( $10 mV_{pp}$ ). To understand how  $V_{diodc}$  varies with the input current and output voltage, you will also need to derive an expression for  $V_{diodc}$  as a function of  $I_{light}$  and  $V_1$ .

The second stage is called a limiting or saturating amplifier. This high-gain CMOS stage amplifies the small voltage  $V_1$ . For maximum amplification,  $V_1$  should be in the high gain region of inverter I2. The open-loop voltage gain of the limiting amplifier  $A_{v2}$  should be large enough to ensure that  $V_1$  is amplified to full logic levels. To scale  $0.1 V_{pp}$  at node  $n_1$  to  $5 V_{pp}$  at node  $n_2$  requires a gain of 50. Since the gain away from the midpoint of the inverter will be less than the maximum gain  $A_{v2}$ , the specification is  $|A_{v2}| \geq 90$ .

The output CMOS stage drives both the wire capacitance and the input capacitance of the digital signal processing circuits. This can be modelled as a constant 50 fF load capacitor. The output driver should be high speed to maximize the frequency at which the receiver can operate. Since the output will be routed to the digital side of the chip, it should also have good noise margins. Specifically,  $t_{PHL}, t_{PLH} \leq 0.5 \text{ nsec}$  and  $NM_L, NM_H \geq 1.4 \text{ V}$  between the input and output of inverter I3.

Power consumption is a big differentiator in system design. To get the edge over competitors, power should be minimized. Since the input and output voltages of inverter I1 are so small, I1 will stay in the high gain region, dissipating static power. To simplify your hand calculations, calculate the power dissipated in I1 when  $I_{light}=0$ . There is also dynamic power required to charge and discharge the parasitic and load capacitance at nodes  $n_1$ ,  $n_2$  and  $n_{out}$ . The total power consumption should