

UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
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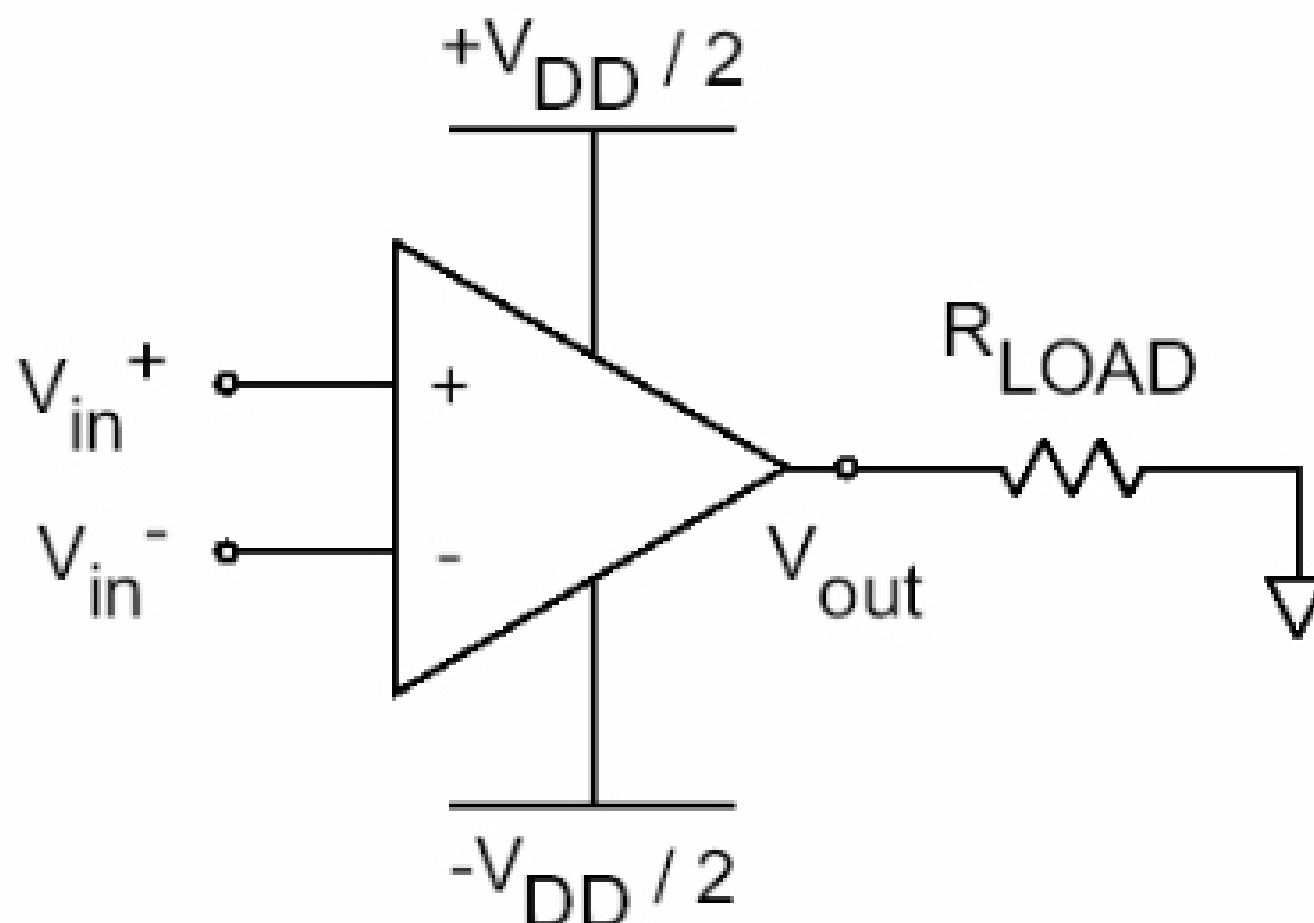
Project 1
(Due 11/05/03)

EECS 140
Fall 2003

This is an individual project. Everybody should turn in a project report.

1. Design Objective

The objective of this project is to design an operational amplifier having a differential input and a single ended output and with the following specifications:



Process	0.13μm
V_{DD}	1.2V
A_{dm}	≥ 10000
A_{cm}	≤ 0.02
R_{LOAD}	50Ω
V_{ICM,max} - V_{ICM,min}	$\geq 0.4V$
V_{ID}	$\leq 100\mu V$
V_{out,pp}	$\geq 0.8V$
V_{Dsat}	$\geq 100mV$
Total Power dissipation	Minimize
Area	Minimize

You are free to choose the midpoint of the common mode input range.

The requirement of $V_{ID} \leq 100\mu\text{V}$ means that differential mode offset voltage is less than 100 μV . For a differential offset input and a common mode input at the midpoint of the common mode input range, the output should be 0 V under nominal supply conditions.

Your circuit should only use the positive $+V_{DD}/2$ and the negative $-V_{DD}/2$ supply.

The design specifications should be met under a variation of the supply voltages of 10 % (higher or lower than the nominal voltage).

The available components are: NMOS transistors, PMOS transistors and resistors. Ideal sources can only be used to generate the supply voltages, not to generate bias currents.

Area Calculation

Calculate the area by adding up the gate area ($W*L$) of all the transistors and the area of the resistors. For the transistors, the minimum L is 0.13 μm and the minimum W is 0.25 μm . For the resistors, the minimum W and L are 0.5 μm ; the sheet resistance is 250 Ω /square.

You are allowed to tie the bulk of any transistor to the source instead of to the positive or negative supply, but at the cost of an area penalty. If you choose to tie the bulk to the source, the area of the transistor should be doubled.

Device Models

http://bwrc.eecs.berkeley.edu/classes/ee140/projects/proj1_model.sp

The device models are encapsulated in a sub-circuit; use: