UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Science

R. W. Brodersen	**Project 2**	**EECS 140**
Jianhui Zhang	**(Due 12/08/03)**	**Fall 2003**

You can work in groups of two, or alone. If you work in groups of two, submit only one project report per group. There will be no extra credit for working alone. The project report and the SPICE deck are due on 12/08/03 at 5pm. Submit the the SPICE deck by sending the 'circuit.sp' file to zhangjh@eecs.berkeley.edu in the body of a text email (no html, no attachments). Submit the project report underneath my door in 402 Cory by 5:00 PM on Monday Dec. 8 or at the BWRC.

Design Objective

The goal of this project is to design an operational trans-conductance amplifier to be used in a switched capacitor circuit. The amplifier will have a differential input and a single ended output. Figure 1 shows the feedback configuration for which the OTA has to be designed.

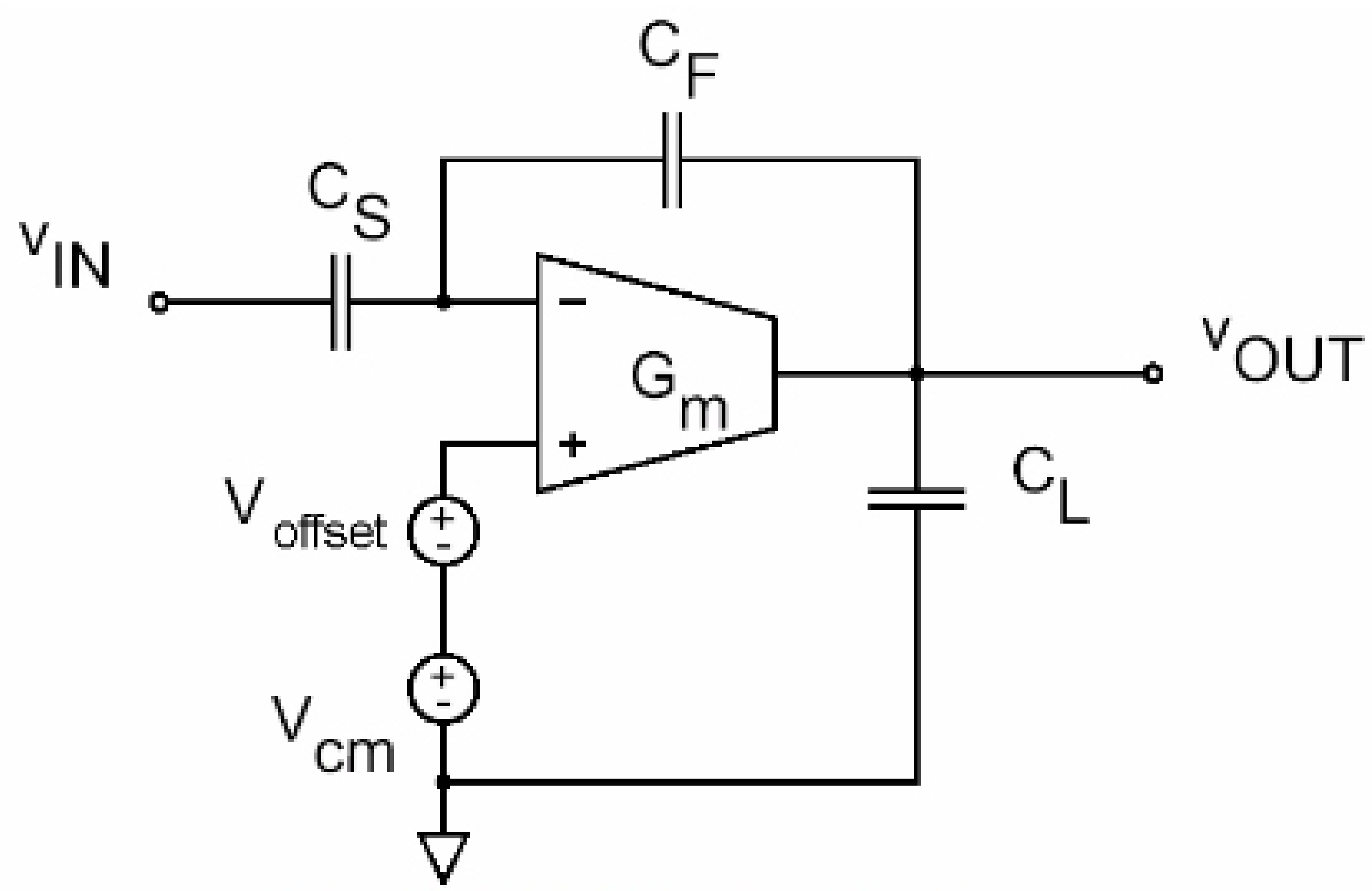

Figure 1 Feedback configuration.

Notice that the amplifier is labeled "**G_m**". It is actually an operational trans-conductance amplifier (OTA), since it does not drive a resistive load, but a capacitive load. The practical implication is that there is no need for an output stage with a low output resistance (which is why the sharp end in the amplifier symbol is missing in Figure 1).

The system specifications are list in Table 1.

Process	0.13µm
VDD	1.2V
Vin	0 to ±0.4 V Step input voltage
t_{settle}	≤ 10ns
Settling accuracy	0.1%
$C_L = C_S$	250 fF
C_F	500 fF
V_{Dsat} of transistors	≥ 100mV
$\lvert V_{offset} \rvert$	≤ 100µV
A_{cm} of amplifier	≤ 0.01
Power Dissipation	Minimized

Table 1 System Specifications

The closed loop gain of the circuit is (very close to) $C_S/C_F = 0.5$. Thus, for a 0.8 peak-to-peak step input voltage, the peak-to-peak output voltage should be 0.4 V and this is the minimum output voltage range of the amplifier.

You are free to choose the common mode reference V_{cm}. The nominal DC output voltage can be any value between -0.4V and +0.4V if it can meet the output voltage swing requirement. You are allowed to connect an input offset voltage in series with the common mode reference to set your output voltage.

The settling is measured for a step at the input going from 0 to ±0.4V. The settling accuracy of 0.1% is specified with respect to the limiting value for $t \rightarrow \infty$. So this 0.1% relates to the dynamic settling error as well as the settling error due to a finite amplifier gain (static settling error).

The constraint on the V_{Dsat}.s should be met for $V_{in+} = V_{in-} = V_{cm}$ (i.e., both inputs to the differential amplifier tied to the common mode reference). The test bench will check for strict compliance with this constraint: if you designed the transistors for a V_{Dsat} of exactly 100 mV, but they are slightly lower in simulation, then you will have to tweak the transistors so that this constraint will be met.

Test benches

Test benches will be made available which will allow you to test all the specifications listed in table 1. The test benches will provide additional tests, such as loop gain. These additional tests are provided to you to debug your circuit, they will not be used to check the performance of your circuit.

Your circuit should only implement the box labeled “G_m” in Figure 1. *Do not include the feedback or load capacitors in your circuit*. In order to use the test benches, your circuit should be in a file named .circuit.sp’ and this file should have the following structure:

```
.param VIC = < your common mode bias voltage >
.subckt ota inp inn out vdd vss
< your circuit >
.ends
```

‘inp’ and ‘inn’ are the positive and negative input respectively. ‘out’ is the output. ‘vdd’ and ‘vss’ are the positive and negative supplies.

Device Models

http://bwrc.eecs.berkeley.edu/classes/ee140/projects/proj2_model.sp

The device models are encapsulated in a sub-circuit; use: