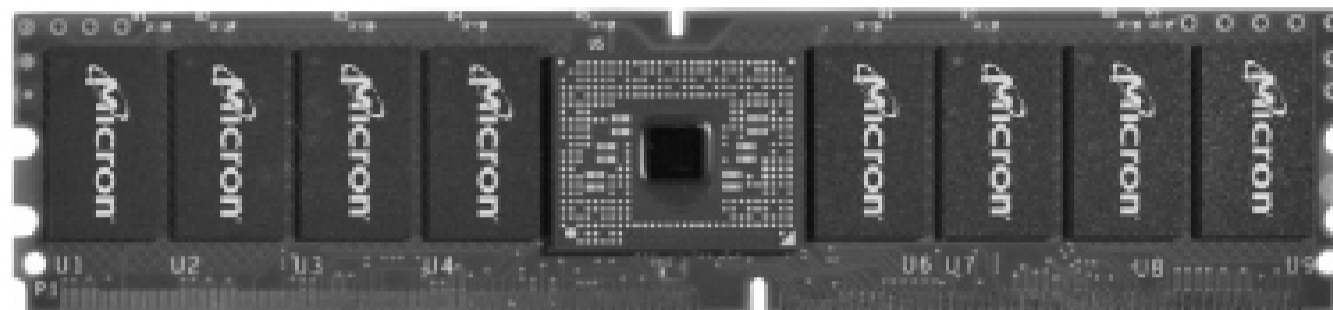


DRAM

Memory Access Protocols

develop generic model for thinking about timing

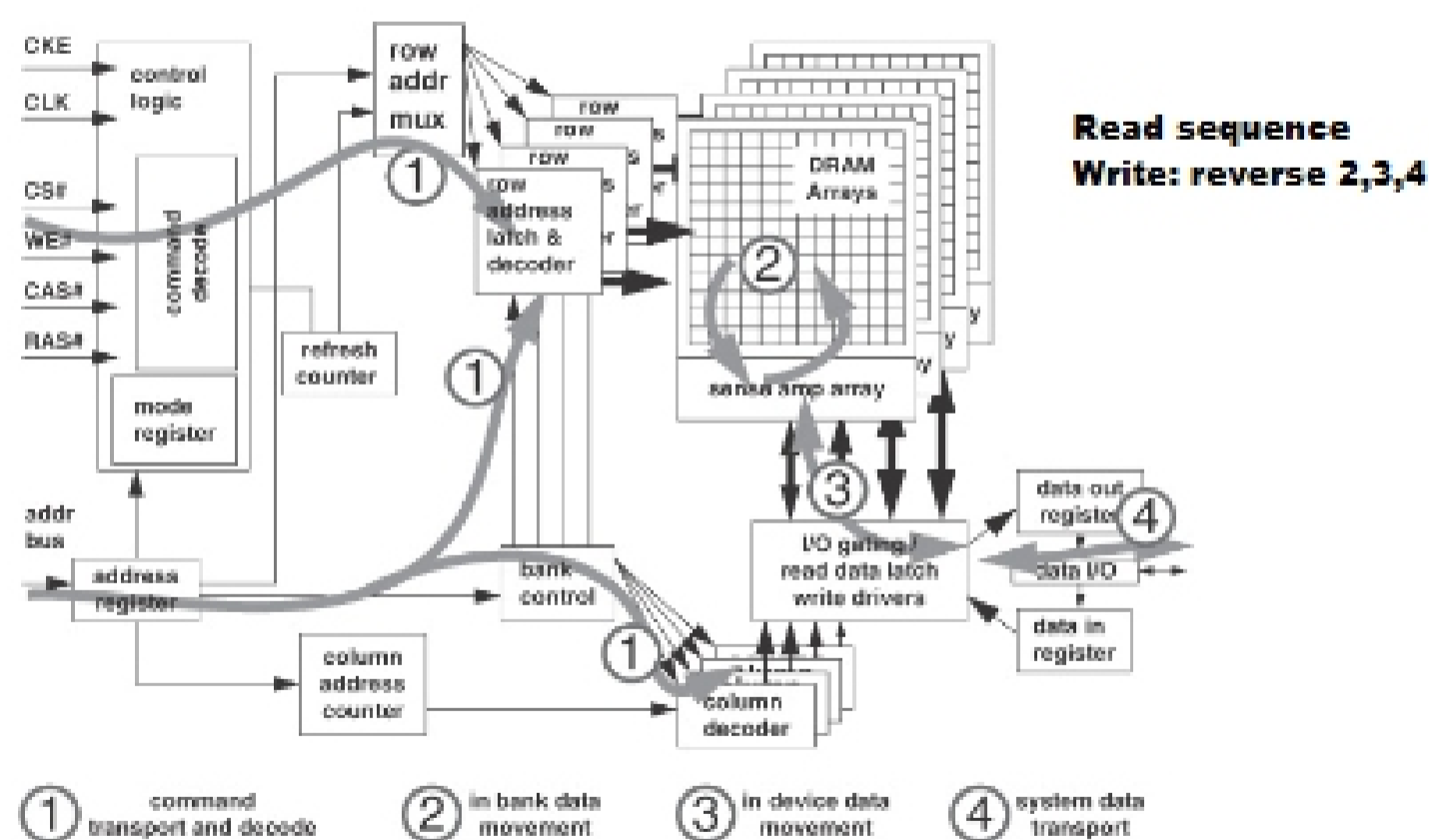


Reference: "Memory Systems: Cache, DRAM, Disk" & Micron website

Bruce Jacob, Spencer Ng, & David Wang

Today's material & any uncredited diagram came from chapter 11

Generic Structure



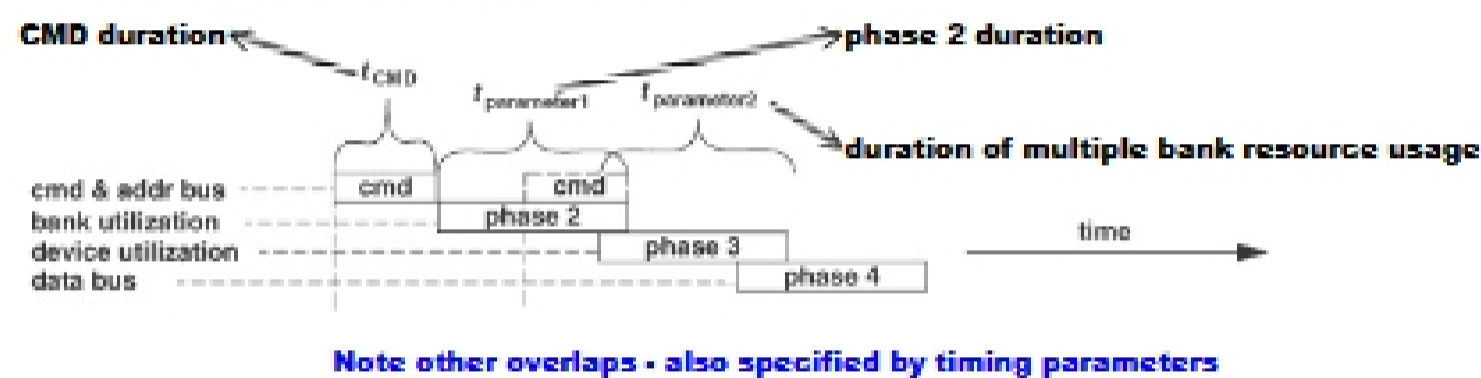
Abstract Command Structure

- Reality

- huge variety of command sequences possible
 - » all with heavily constrained timing issues
 - 2 roles of timing
 - 1) physical: latency, set-up and hold, signal integrity, lane retiming
 - 2) power: limit concurrency to stay under thermal/power ceiling

- Start simple

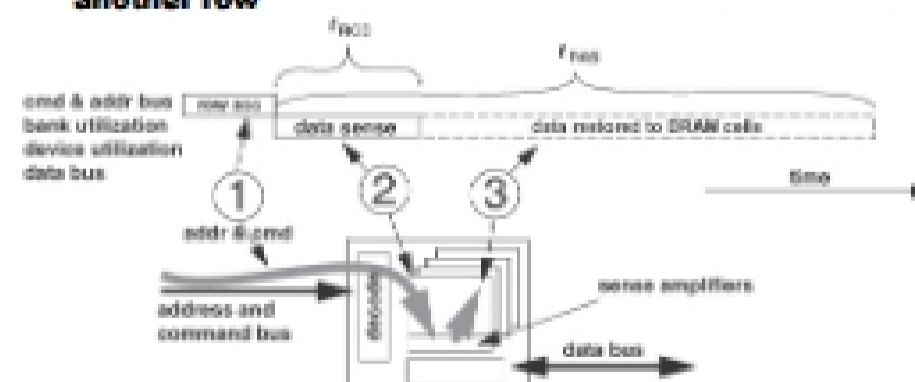
- command & phase overlap



Row Access Command

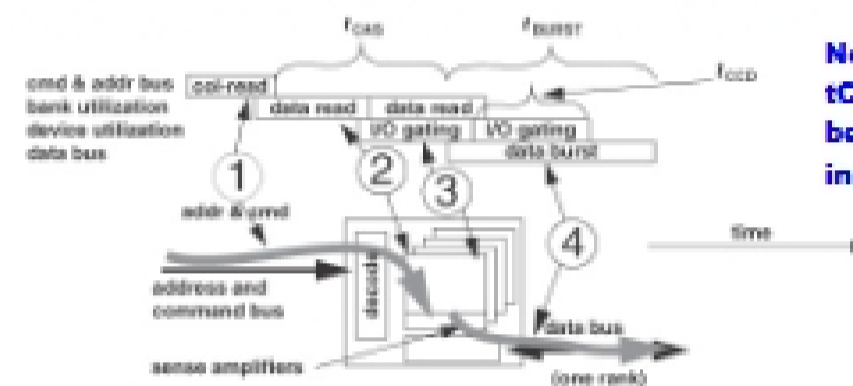
- Row activation

- move data from the mats to sense amps and restore the mats
 - » controlled by 2 timing parameters
 - t_{RCD} - row command delay
 - time to move the data from the mats to the sense amps
 - after a RAS command + t_{RCD} : column reads or writes can commence
 - t_{RAS} - interval between a RAS command and row restore
 - after a RAS command + t_{RAS} sense amps can be precharged to activate another row



Column Read Command

- **Bank specific**
 - **move data from sense amps through I/O's to the Mem_Ctrl**
 - » **3 timing parameters**
 - t_{CAS} (or t_{CL}) • **column address strobe**
 - time between col-rd (CAS) command and data valid on the data bus
 - DDRx devices do this in short continuous bursts
 - t_{CCD} • **minimum column to column command delay due to burst I/O gating**
 - 1 cycle for DDR, 2 cycles for DDR2, 4 cycles for DDR3, etc.
 - t_{BURST} • **duration of the data burst on the bus**



Note: some devices have $t_{CCD} > t_{BURST}$ where t_{CCD} becomes the limiting factor in what can happen next

Column Write Command

- **Move data from mem_ctrl to sense amps**
 - **timing parameters**
 - » t_{CWD} • **delay between col-write and data valid on bus from mem-ctrl**
 - some per device differences differences
 - SDRAM: t_{CWD} is typically 0
 - DDR - typically 1 memory clock cycle
 - DDR2 - t_{CAS} - 1 cycle
 - DDR3 - t_{CWD} is programmable
 - » **Other parameters control a subsequent command's timing**
 - t_{WTR} • **write to read delay**
 - end of write data burst to column read command delay
 - t_{WR} • **write recovery delay**
 - min. interval between end of a write data burst and start of a precharge command
 - I/O gating allowed to overdrive sense amps prior to col-rd-cmdn (mat restore)
 - t_{CMD} • **time command occupies command bus**