

**PROBLEM SET #9**

*Issued: Tuesday, April 7, 2009*

*Due: Tuesday, April 14, 2009, 5:00 p.m. in the EE 140 homework box in 240 Cory*

1. An amplifier has low-frequency forward gain of 40,000, and its transfer function has three negative real poles with magnitudes 2 kHz, 200 kHz, and 4 MHz.
  - (a) If this amplifier is connected in a feedback loop with a constant feedback factor  $f$  and with low-frequency gain  $A_0=400$ , estimate the phase margin;
  - (b) Repeat (a) if  $A_0=200$  and then 100.
  
2. The amplifier  $a(s)$  is has DC gain of 10,000 and three real negative poles. The pole frequencies of the first and the third pole are 1 kHz and 200 MHz, respectively.
  - (a) If  $R_1=R_2$  find the location of the second pole such that the feedback amplifier shown in Figure PS9-2 is stable with a phase margin of  $60^\circ$ . Neglect the input impedance of the amplifier.
  - (b) Write the transfer function in as a function of the complex variable  $s$  and draw Bode plots for the open-loop amplifier gain  $a(s)$  and the closed-loop gain  $A(s)$ .
  - (c) What is the new phase margin if:
    - i. In addition to the three poles the amplifier  $a(s)$  has one real right half-plane zero at the frequency of the second pole.
    - ii. In addition to the three poles the amplifier  $a(s)$  has one real left half-plane zero at the frequency of the second pole.
    - iii. The closed-loop amplifier  $A(s)$  is configured as a unity gain buffer.
    - iv.  $R_1=9R_2$ .

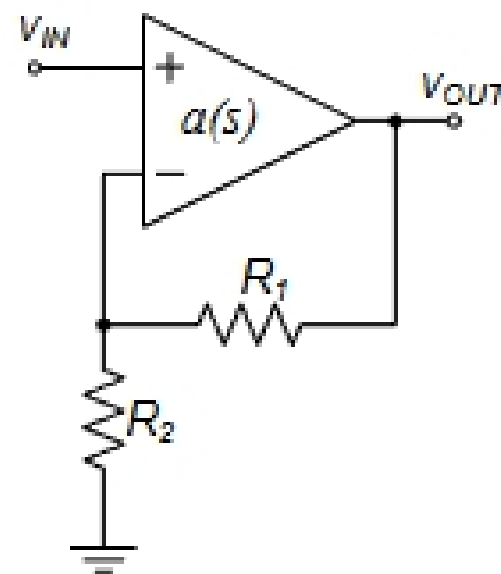


Figure PS9-2

3. Razavi, Chapter 10: Problem 10.4.

4. In the amplifier shown in Figure PS9-4 transistors  $M_3$ - $M_8$  are biased with  $V_{ov}=200\text{mV}$ . The gates of  $M_3$  and  $M_4$  are biased to allow the maximum undistorted sinusoidal signal at the output. Calculate all currents, channel widths and the value of capacitor  $C_c$  so that the amplifier has a DC gain of 20, a unity gain frequency of 50MHz, and a phase margin of  $60^\circ$  when placed in unity gain closed-loop feedback. All transistors have the same channel length. Neglect all parasitic capacitances in this problem.

$$V_{DD} = 3V, R_L = 10k\Omega, C_L = 5pF$$

$$V_{th0,n} = 0.5V, \mu_n C_{ox} = 250 \frac{\mu A}{V^2}, L = 0.5\mu m, \lambda = 0, \gamma = 0, L_d = 0$$

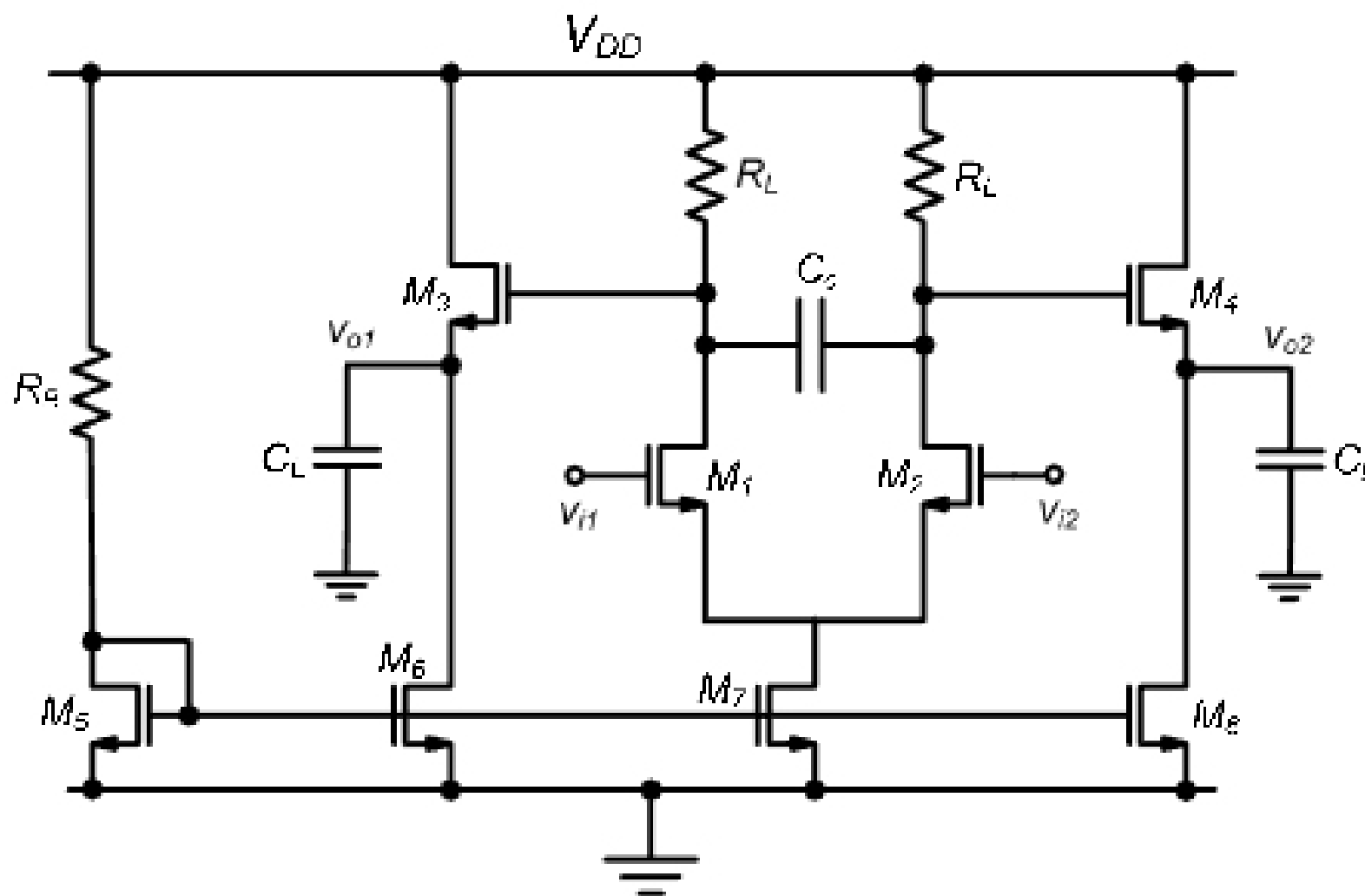


Figure PS9-4