EECS 150 - Components and Design Techniques for Digital Systems

Lec 15 – Storage: Regs, SRAM, ROM

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Review: Timing

- All gates have delays
  - RC delay in driving the output
- Wires are distributed RCs
  - Delays goes with the square of the length
- Source circuits determines strength
  - Serial vs parallel
- Delays in combinational logic determine by
  - Input delay
  - Path length
  - Delay of each gate along the path
  - Worst case over all possible input-output paths
- Setup and CLK-Q determined by the two latches in flipflop
- Clock cycle : $T_{cycle} \geq T_{CL}+T_{setup}+T_{clk \rightarrow Q}$ + worst case skew

- Delays can introduce glitches in combinational logic

Outline

- Memory concepts
- Register Files
- SRAM
- SRAM Access
- Multiported Memories
  - FIFOS
- ROM, EPROM, FLASH
- Relationship to Comb. Logic