

# CPEG 222 Spring 2014

## Homework 2

**Due April 23 at noon (through sakai)**

**Note: To receive full credit, please show your steps and put comments for your code.**

1. The following code is written in C, where array elements within the same row are stored contiguously.

```
for (I=0; I<8; I++)
    for (J=0; J<8000; J++)
        A[I][J]=B[I][0]+A[J][I];
```

- a) References to which variables exhibit temporal locality? References to which variables exhibit spatial locality? Please give a brief explanation.
- b) Now let us switch the inner and outer loop order, as shown below. References to which variables exhibit temporal locality? References to which variables exhibit spatial locality? Please give a brief explanation.

```
for (J=0; J<8000; J++)
    for (I=0; I<8; I++)
        A[I][J]=B[I][0]+A[J][I];
```

2. We have studied both hard disk and Flash drive in class. Use online or library resources, compare their latency, throughput, energy for read and write operations. Also compare their standby energy, capacity and cost. Summarize your answer in a table.
3. The following describes a computer system: What is the bottleneck in the following system setup, the CPU, memory bus, or the disk set?
  - The clock rate is 3GHz.
  - The maximum sustained transfer rate of the memory bus is 640MB/sec.
  - The user program continuously performs reads of 64KB blocks, and requires 2 million cycles to process each block.
  - The operating system requires 1 million cycles of overhead for each I/O operation.
  - The read/write bandwidth of the disk controller and the disk drives is 64MB/sec, disk average seek plus rotational latency is 9ms.
  - There are 5 disks attached to the bus each with its own controller. (Assume that each disk can be controlled independently and ignore disk conflicts.)
4. Assume that main memory accesses take 200ns and that memory accesses are 30% of all instructions. The following table shows data for level 1 (L1) caches attached to two processors, P1 and P2.

|    | L1 Size | L1 Miss Rate | L1 Hit Time |
|----|---------|--------------|-------------|
| P1 | 8KB     | 3.6%         | 1ns         |
| P2 | 16KB    | 2.8%         | 1.8ns       |

- a) Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?
  - b) What is the average memory access time (AMAT) for P1 and P2?
  - c) Assume both processors have the same instruction set and a base CPI of 1.0 (i.e., it takes 1 clock cycle to execute 1 instruction) without any memory stalls, what is the total CPI for P1 and P2 when memory stall is considered? Which processor is faster?
5. Caches use the middle range of address bits as the set index and the high order bits as the tag. Why is this done? How might cache performance be affected if the middle bits were used as the tag and the high order bits were used as the set index?
6. Design a 128KB direct-mapped data cache that uses a 32-bit address and 16 bytes per block. Calculate the following:
- a) How many bits are used for the byte offset?
  - b) How many bits are used for the set (index) field?
  - c) How many bits are used for the tag?