

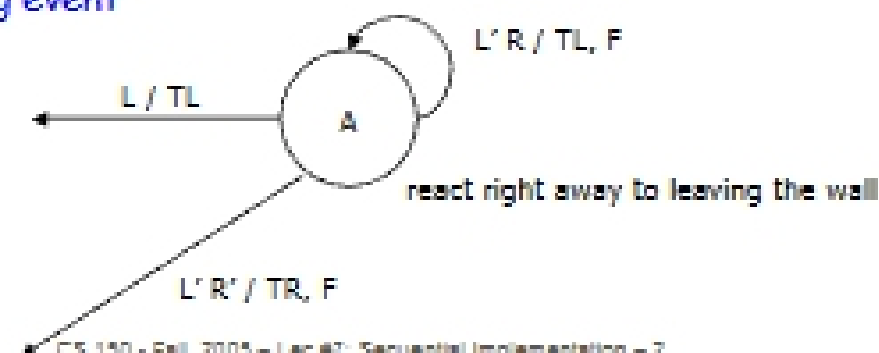
Sequential Logic Implementation

- Models for representing sequential circuits
 - Abstraction of sequential elements
 - Finite state machines and their state diagrams
 - Inputs/outputs
 - Mealy, Moore, and synchronous Mealy machines
- Finite state machine design procedure
 - Verilog specification
 - Deriving state diagram
 - Deriving state transition table
 - Determining next state and output functions
 - Implementing combinational logic

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Mealy vs. Moore Machines

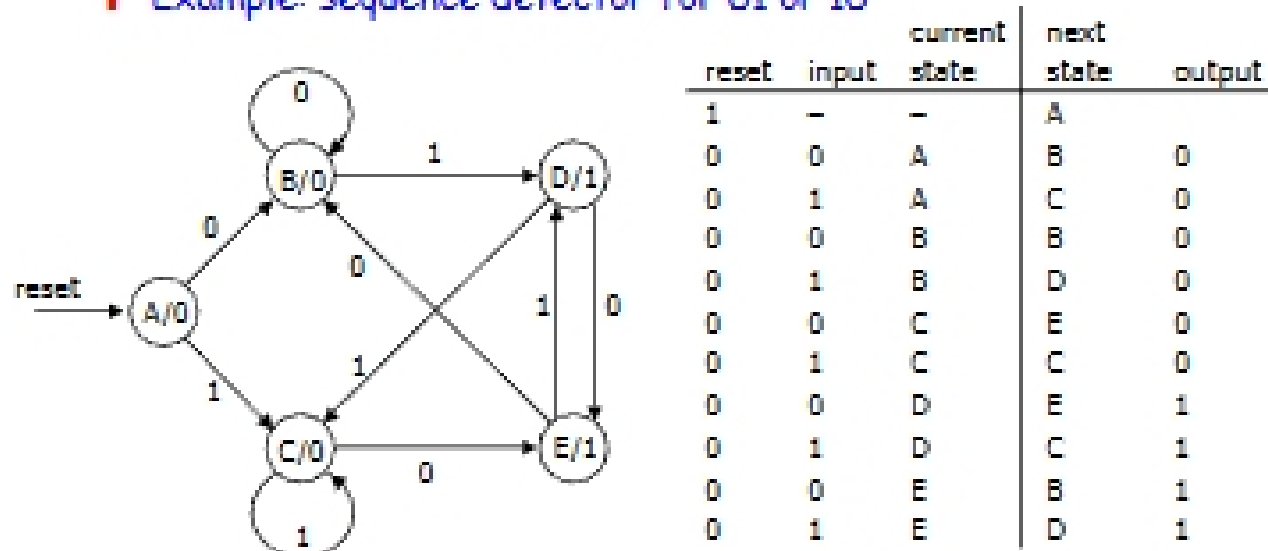
- Moore: outputs depend on current state only
- Mealy: outputs depend on current state and inputs
- Ant brain is a Moore Machine
 - Output does not react immediately to input change
- We could have specified a Mealy FSM
 - Outputs have immediate reaction to inputs
 - As inputs change, so does next state, doesn't commit until clocking event



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Specifying Outputs for a Moore Machine

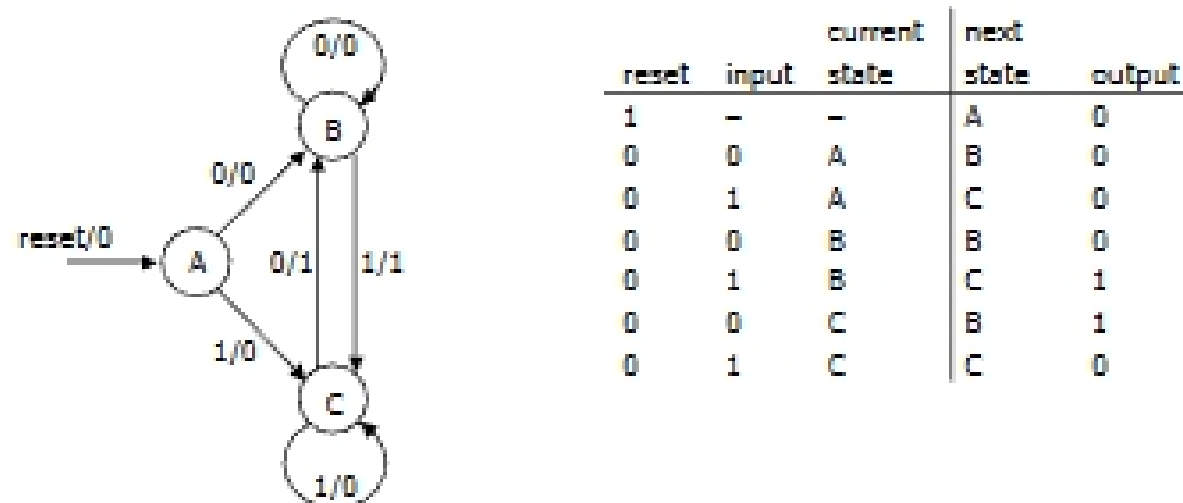
- Output is only function of state
 - Specify in state bubble in state diagram
 - Example: sequence detector for 01 or 10



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Specifying Outputs for a Mealy Machine

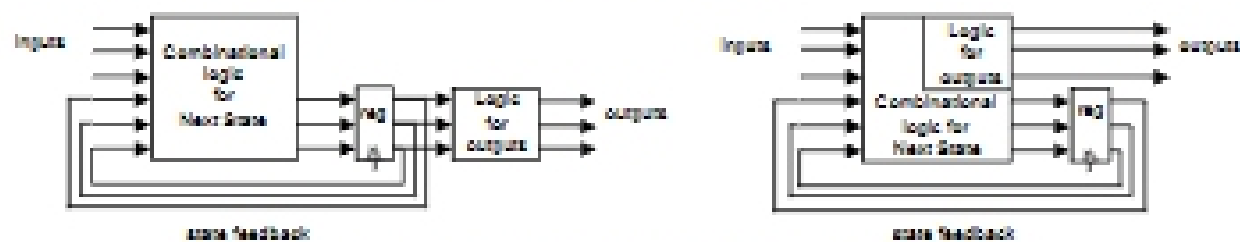
- Output is function of state and inputs
 - Specify output on transition arc between states
 - Example: sequence detector for 01 or 10



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Comparison of Mealy and Moore Machines

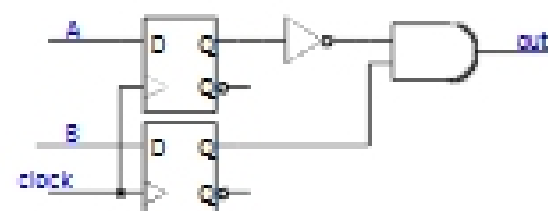
- Mealy Machines tend to have less states
 - Different outputs on arcs (n^2) rather than states (n)
- Moore Machines are safer to use
 - Outputs change at clock edge (always one cycle later)
 - In Mealy machines, input change can cause output change as soon as logic is done - a big problem when two machines are interconnected - asynchronous feedback
- Mealy Machines react faster to inputs
 - React in same cycle - don't need to wait for clock
 - In Moore machines, more logic may be necessary to decode state into outputs - more gate delays after



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Mealy and Moore Examples

- Recognize $A, B = 0, 1$
 - Mealy or Moore?



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