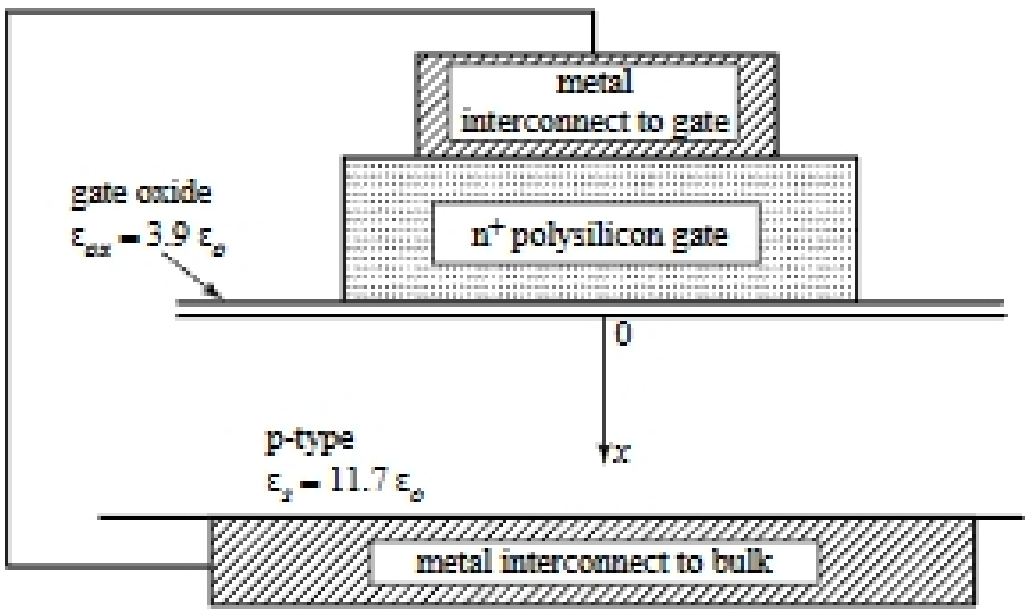
I. The MOS Capacitor in Thermal Equilibrium

A. Introduction

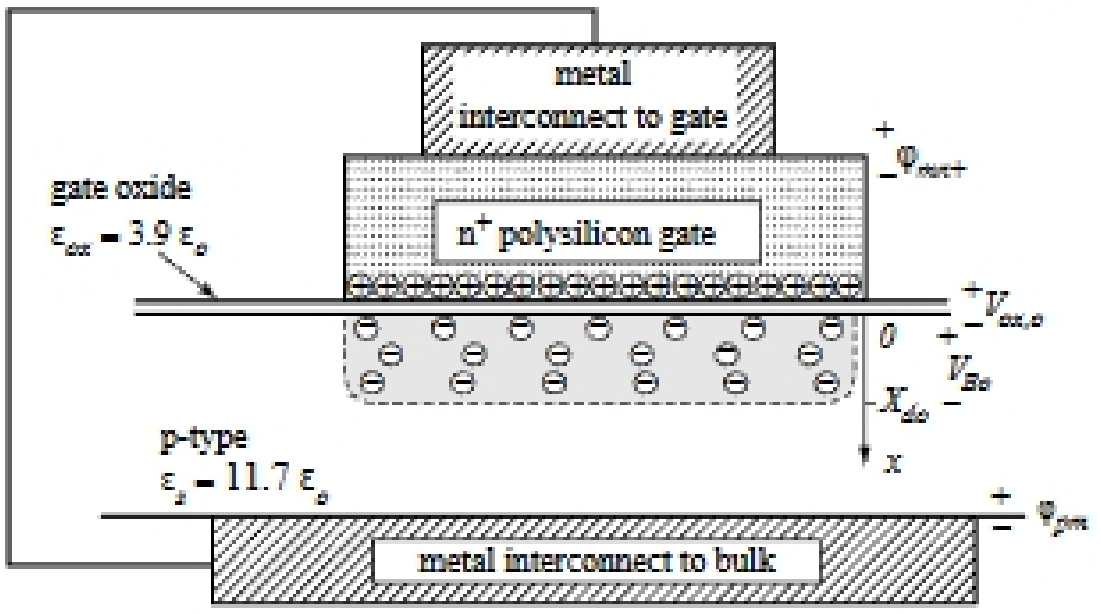


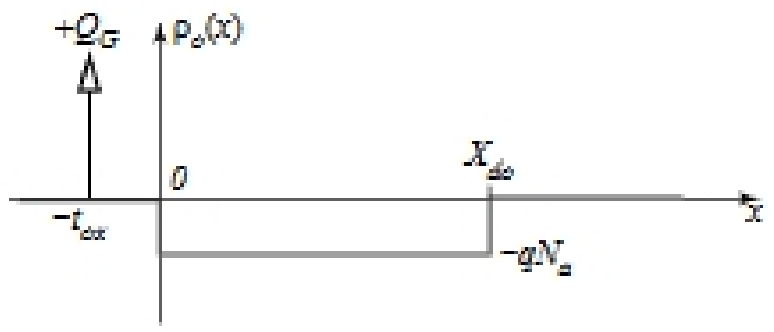
- Oxide = SiO_2 ... a near-perfect insulator.
- Assume zero charge in the oxide, electric field is constant and potential is linear in the oxide.
- n^+ polysilicon has a potential which is the maximum possible in silicon:

$$\varphi_{n+} = 550 \text{ mV}$$

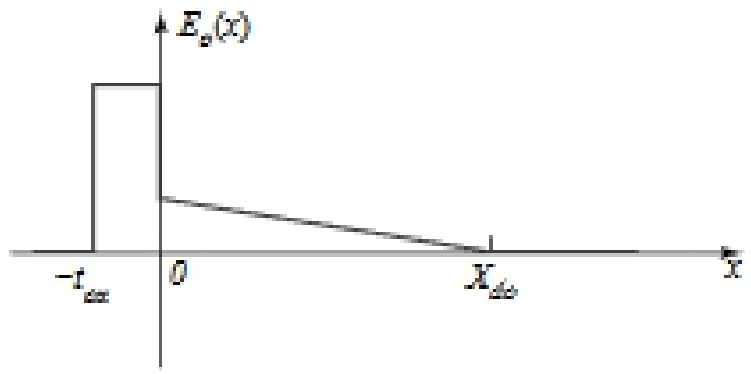
- Example parameters t_{ox}=15nm=150A $N_a = 10^{17}$ cm-3
- φ_p = -420 mV
- The *surface potential* φ_s is the potential at the S_i/S_iO_2 interfaceg
- Strategy: same as pn junction electrostatics: first thermal equilibrium, then with an applied bias.

B. Thermal Equilibrium MOS Electrostatics - Qualitative

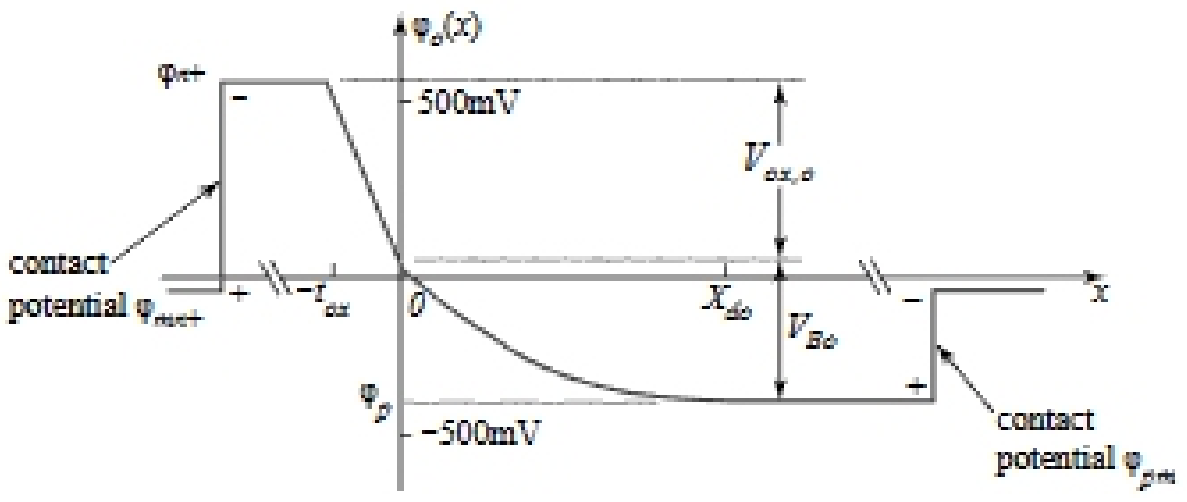




(a)



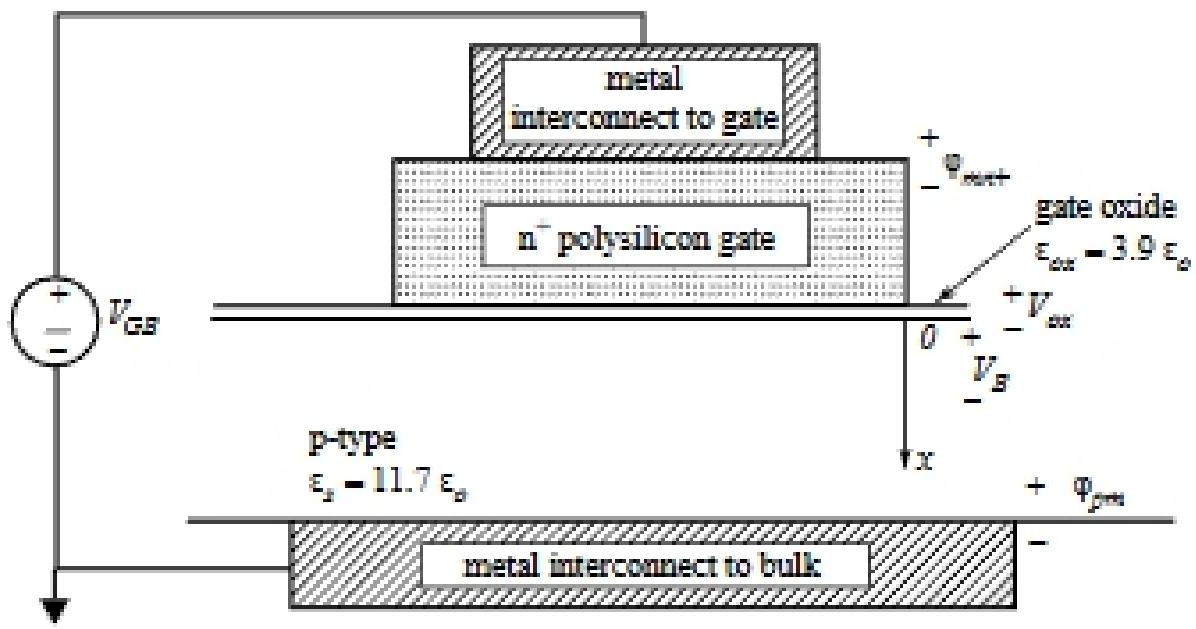
(b)



II. MOS Capacitor under Bias

A. Introduction

- No steady-state current between the n^+ poly gate and the substrate.
- $J_n = 0$ and $J_p = 0$
- Absence of current implies that we can relate potential to carrier concentration in the silicon substrate.



- Flatband condition: cancel built-in drop by applying

$$V_{GB} = -(\varphi_{n+} - \varphi_p) = V_{FB}$$

$$V_{FB} = \text{-970 mV for } N_a = 10^{17}\ \text{cm}^{-3}$$

- For $V_{GB} = V_{FB}$, the internal potential is constant through the structure since both the gate and the p-type substrate have the same potential.