Tutorial: ISE 10.1i and the Spartan3e Board

v1.0

This tutorial will show you how to:

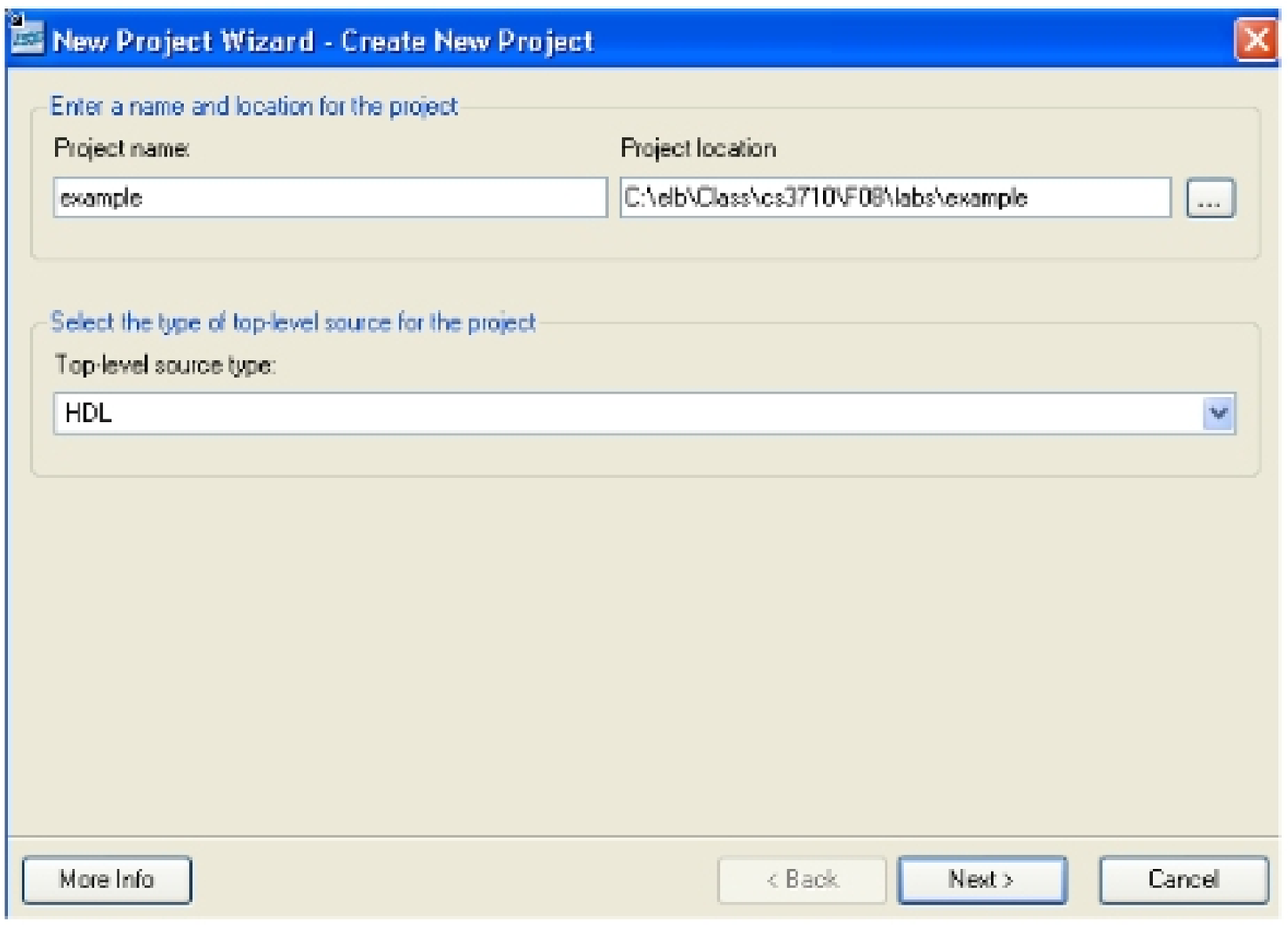
- Use a combination of schematics and Verilog to specify a design
- Simulate that design
- Define pin constraints for the FPGA (.ucf file)
- Synthesize the design for the FPGA board
- Generate a bit file
- Load that bit file onto the Spartan3e board in your lab kit

I assume that you're using a DSL lab machine, or that you've installed Xilinx ISE 10.1i on your own machine. This tutorial is specifically for the Spartan3e board. The programming procedure is different than for the older Spartan2 boards from Xess.

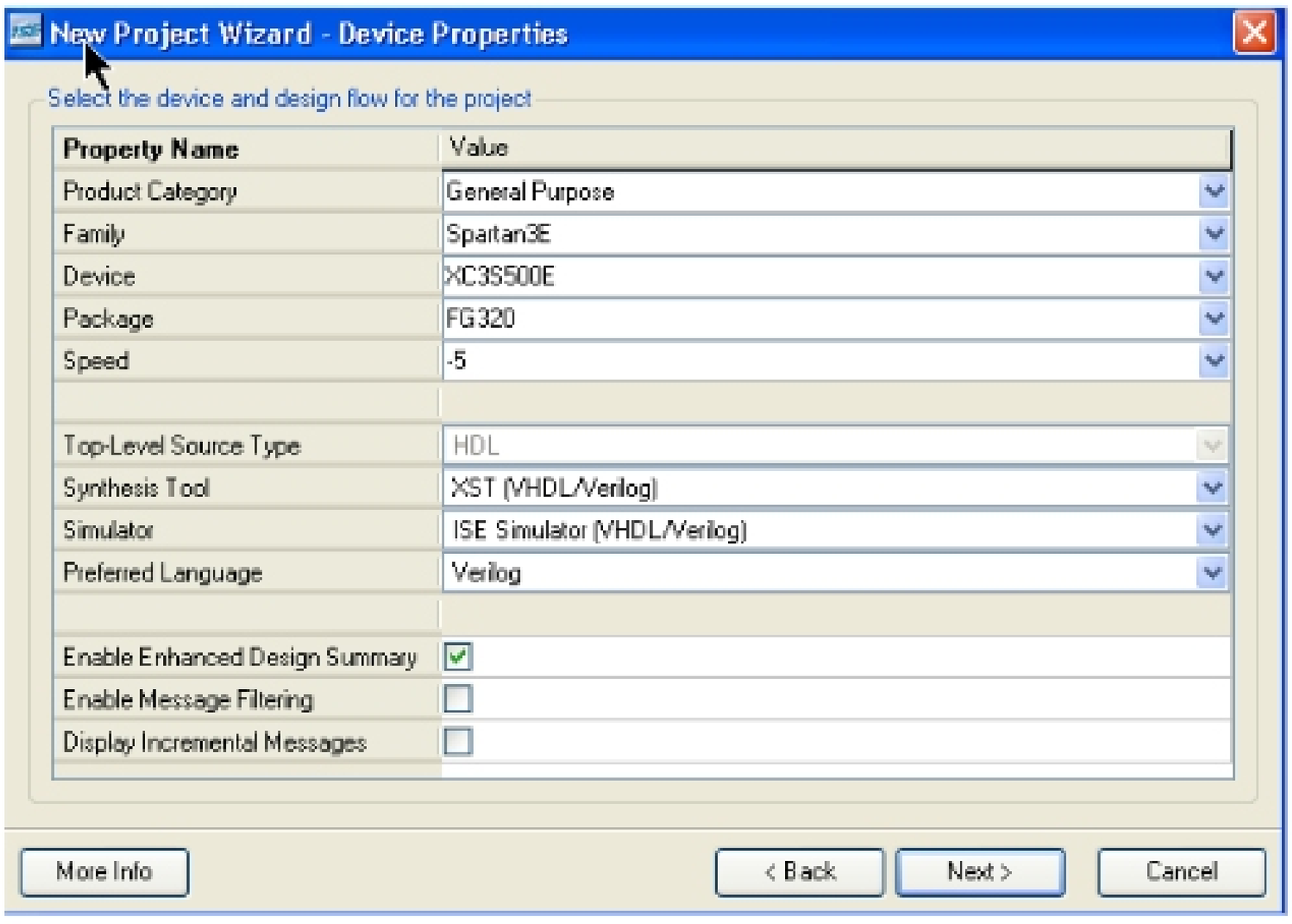
Setting up a New Project and specifying a circuit in Verilog

1. Start the ISE 10.1 tool from Xilinx.

2. Create a new project. The Create New Project wizard will prompt you for a location for your project. Note that by default this will be in the ISE folder the very first time you start up. You'll probably want to change this to something in your own folder tree.

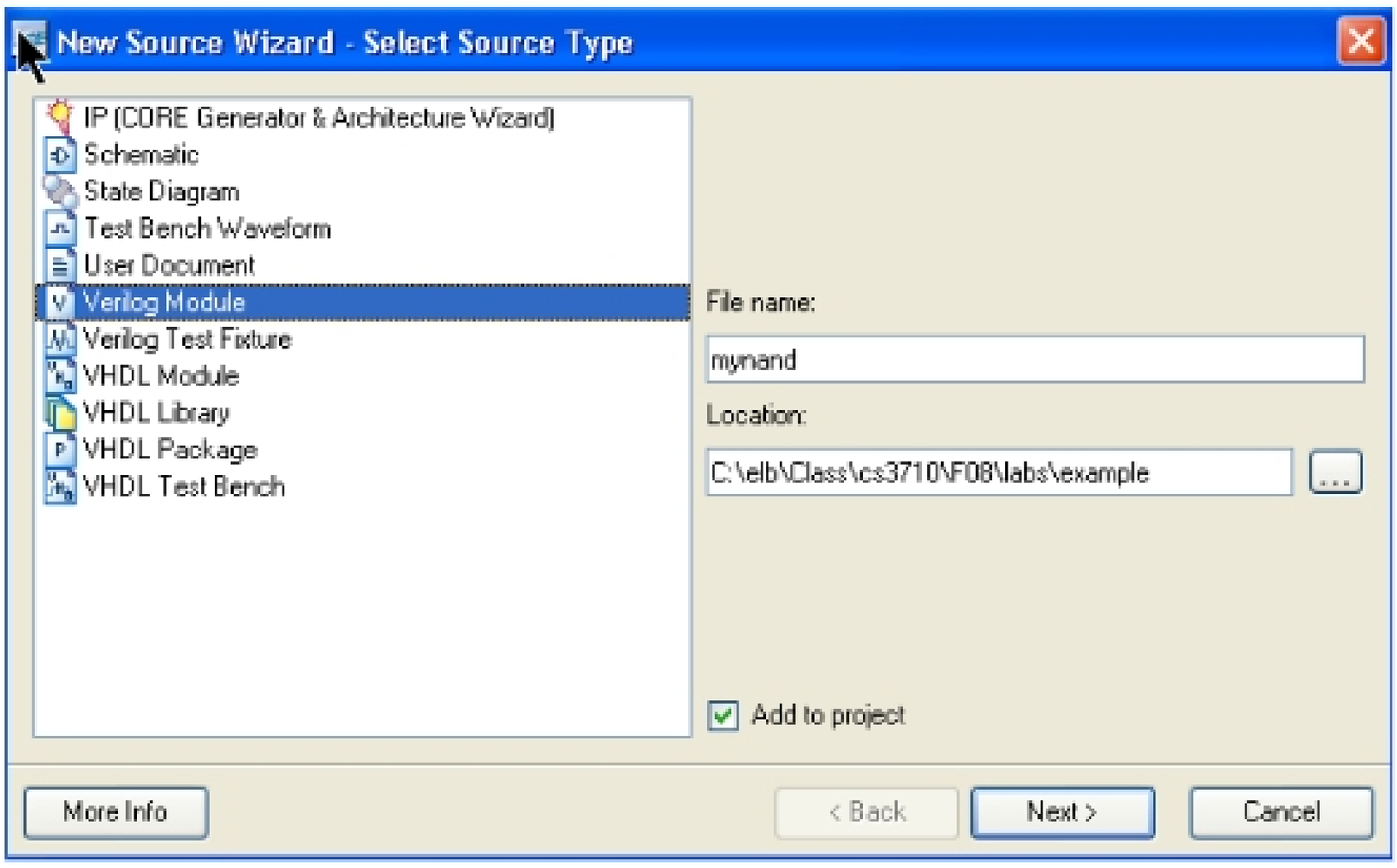


3. On the second page of the Create New Project dialog, make *sure* that you use the **Spartan3e** Device Family, **XC3S500** Device, **FG320** Package, **-5** Speed Grade. You can also specify **HDL** as the Top-Level Source Type with **XST** as the Synthesis Tool, **ISE** as the Simulator, and **Verilog** as the language. These aren't critical, but they do save time later.



4. You can skip the other parts of the dialog, or you can use them to create new Verilog file templates for your project. I usually just skip them and create my own files later.

5. Now you want to open a new source file. Use the **Project►NewSource** menu choice. This first one will be a Verilog file so make sure you've selected **Verilog Module** as the type and give it a name. I'm calling my example **mynand**.



6. When you press **Next** you'll get a dialog box that lets you define the inputs and outputs of your new module. I'm adding two inputs (**A** and **B**), and one output named **Y**. Remember that Verilog is case sensitive!