

# Tutorial: ISE 12.2 and the Spartan3e Board

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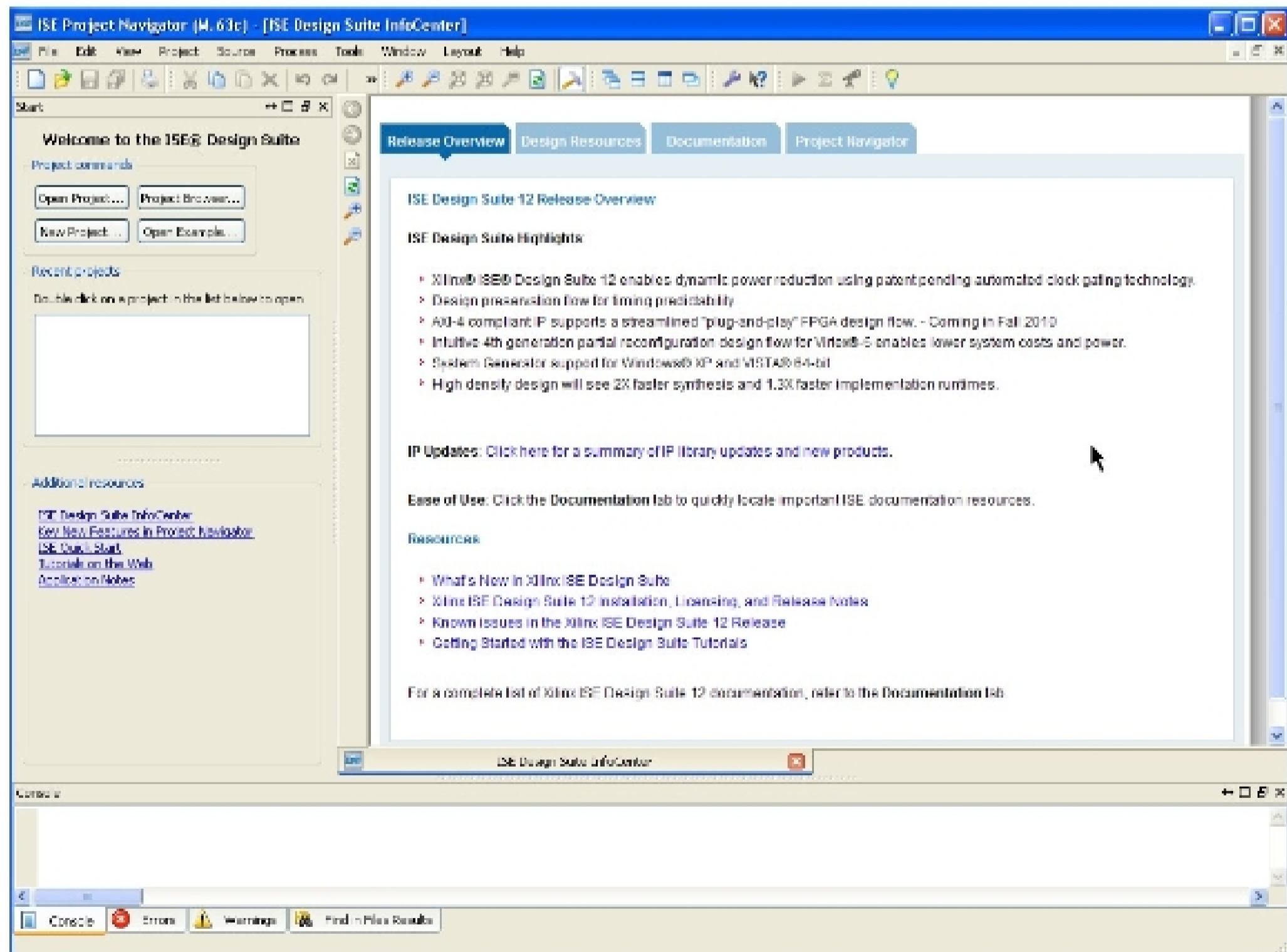
## This tutorial will show you how to:

- Use a combination of schematics and Verilog to specify a design
- Simulate that design
- Define pin constraints for the FPGA (.ucf file)
- Synthesize the design for the FPGA board
- Generate a bit file
- Load that bit file onto the Spartan3e board in your lab kit

I assume that you're using a DSL lab machine, or that you've installed Xilinx ISE 12.2 on your own machine. This tutorial is specifically for the Spartan3e board. The programming procedure is different than for the older Spartan2 boards from Xess.

## Setting up a New Project and specifying a circuit in Verilog

1. Start the ISE 12.2 tool from Xilinx.



2. Create a new project. The Create New Project wizard will prompt you for a location for your project. Note that by default this will be in the ISE folder the very first time you start up. You'll probably want to change this to something in your own folder tree.

**New Project Wizard**

**Create New Project**  
Specify project location and type.

Enter a name, locations, and comment for the project

Name: example

Location: C:\Documents and Settings\Erik\My Documents\Xilinx12-2\example ...

Working Directory: C:\Documents and Settings\Erik\My Documents\Xilinx12-2\example ...

Description: example project

Select the type of top-level source for the project

Top-level source type: Schematic

More Info Next > Cancel

3. On the second page of the Create New Project dialog, make *sure* that you use the **Spartan3e** Device Family, **XC3S500** Device, **FG320** Package, **-5** Speed Grade. You can also specify **HDL** as the Top-Level Source Type with **XST** as the Synthesis Tool, **ISE** as the Simulator, and **Verilog** as the language. These aren't critical, but they do save time later.

**New Project Wizard**

**Project Settings**  
Specify device and project properties.

Select the device and design flow for the project

Property Name	Value
Product Category	General Purpose
<b>Family</b>	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-5
Top-Level Source Type	Schematic
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

You'll see a confirmation screen after setting things up: