

Data Hazards and Stalls

- Data hazards and forwarding
- Data Hazards and Stalls

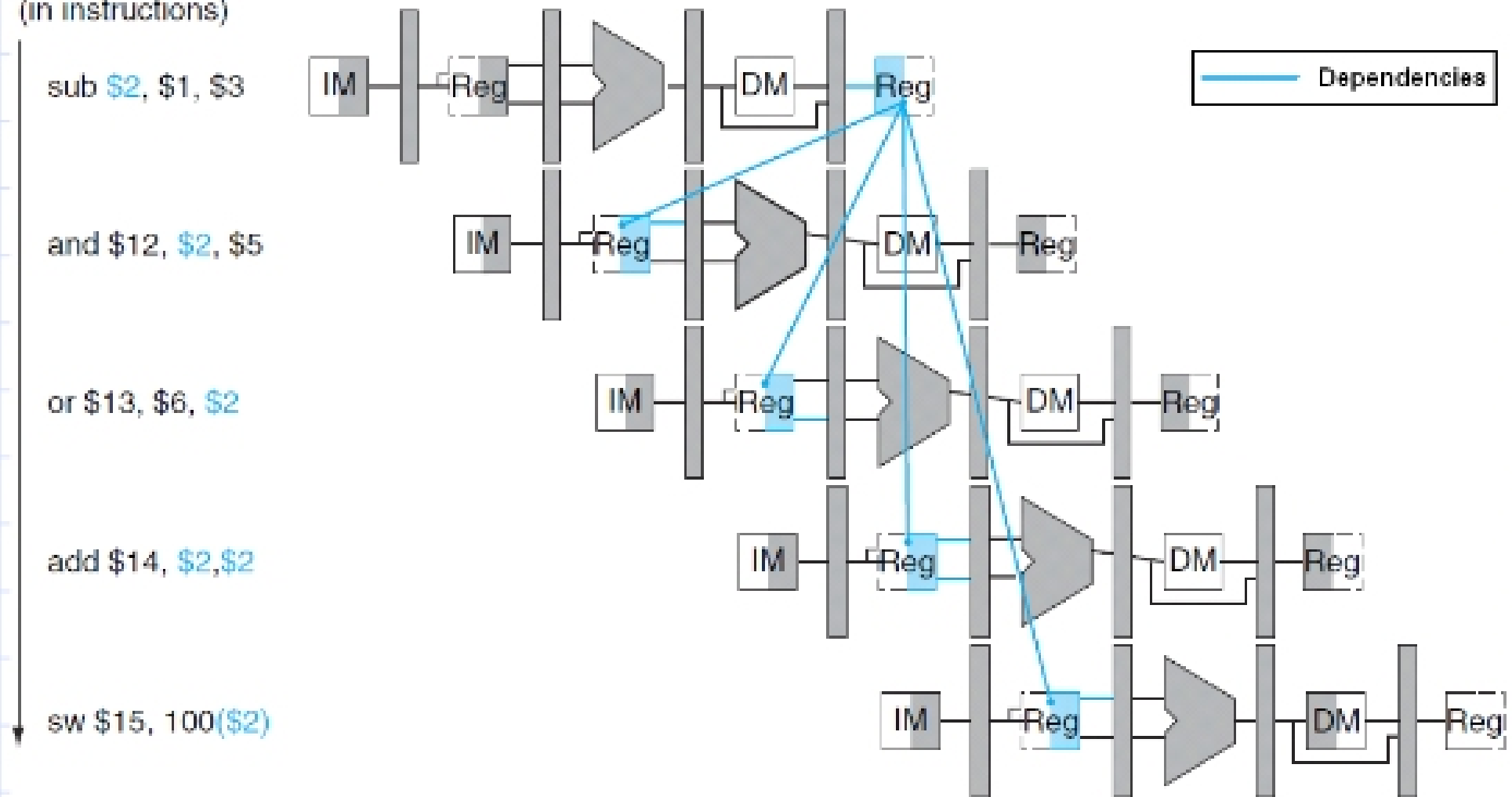
An Example

<i>sub</i>	\$2, \$1, \$3	# Register \$2 written by sub
<i>and</i>	\$12, \$2, \$5	# 1st operand (\$2) depends on sub
<i>or</i>	\$13, \$6, \$2	# 2nd operand (\$2) depend on sub
<i>add</i>	\$14, \$2, \$2	# 1st (\$2) & 2nd (\$2) depend on sub
<i>sw</i>	\$15, 100(\$2)	# Index (\$2) depends on sub

Assuming that register R2 = 10 initially. And the sub instruction will result in R2 = -20.

	Time (in clock cycles) →								
Value of register \$2:	CC 1	CC 2	CC 3	CC 4	CC 5	CC 6	CC 7	CC 8	CC 9
	10	10	10	10	10/-20	-20	-20	-20	-20

Program execution order (in instructions)



See P&H Fig. 6.28 3rd Ed or 4.52 4th Ed

Pipelined dependencies in a five instruction sequence using simplified datapaths to show the dependencies.

Note: only add and sw get the right value R2 = - 20