EE140 project 2 submission guidelines

1 Project report guidelines

Submit only one project per group. The project report is due Monday, December 9, at noon, at the BWRC. Your project report should include the following sections:

- Discussion of your topology choice: explain why you chose a certain topology and compare your topology with possible alternatives.
- Discussion of your sizing and power minimization strategy: explain how you chose all the W's, L's, V_{Dsat}'s and currents; show your calculations.
- A schematic (drawn by hand) of your circuit, annotated with all the node voltages.

  Provide a table with W, L, V_{Dsat} and I_{DS} for every transistor. For V_{Dsat} and I_{DS}, include both the calculated and the simulated values. You only need to add one entry for every pair of symmetric transistors, such as the transistors in a differential pair.

  Provide a table with every resistor and capacitor in your circuit. You do not have to include the feedback capacitors, only the capacitors you added yourself.
- A table with the results from the testbenches and the power consumption. Explain differences with your hand calculations.
- A plot of the time domain response for a positive input step and a negative input step (testbench 1).
- Comments and conclusion.

DO NOT INCLUDE SPICE LISTINGS IN THE PROJECT REPORT.

2 Circuit submission guidelines

Send an email to `ee140@cory.eecs.berkeley.edu` *with your name(s) in the subject* (i.e. not in the body of the email) and your circuit in the body of

the email. Do not add any comments to the body of the email. Make sure to send the email in *plain text*, not in html.

The body of the email should be the same as the file used to run the testbenches:

```
.param VIC = < your midpoint of the common mode input range >
.subckt ota inp inn out vdd vss
< your circuit >
.ends
```

The subcircuit should be named 'ota' and the order of the input nodes should be: positive input node, negative input node, output node, positive supply, negative supply. You can change the names of the nodes.

Do not add include statements, model statements, simulation statements, supply sources, ... You will loose points if I have to fix up your SPICE deck to make it run.