SYNCHRONOUS DRAM

MT48LC32M4A2 – 8 Meg x 4 x 4 banks
MT48LC16M8A2 – 4 Meg x 8 x 4 banks
MT48LC8M16A2 – 2 Meg x 16 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/dramds

FEATURES

- PC100-, and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Mode; standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS — MARKING

- Configurations
  - 32 Meg x 4 (8 Meg x 4 x 4 banks) — 32M4
  - 16 Meg x 8 (4 Meg x 8 x 4 banks) — 16M8
  - 8 Meg x 16 (2 Meg x 16 x 4 banks) — 8M16
- WRITE Recovery (t_{WR})
  - t_{WR} = "2 CLK"[1] — A2
- Package/Pinout
  - Plastic Package – OCPL[2]
  - 54-pin TSOP II (400 mil) — TG
  - 60-ball FBGA (8mm x 16mm) — FB[3,6]
  - 60-ball FBGA (11mm x 13mm) — FC[3,6]
- Timing (Cycle Time)
  - 10ns @ CL = 2 (PC100) — -8E[3,4,5]
  - 7.5ns @ CL = 3 (PC133) — -75
  - 7.5ns @ CL = 2 (PC133) — -7E
- Self Refresh
  - Standard — None
  - Low power — L
- Operating Temperature Range
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT[3]

Part Number Example:

MT48LC16M8A2TG-7E

NOTE: 1. Refer to Micron Technical Note: TN-48-05.
2. Off-center parting line.
3. Consult Micron for availability.
4. Not recommended for new designs.
5. Shown for PC100 compatability.
6. See page 59 for FBGA Device Marking Table.

PIN ASSIGNMENT (Top View)

54-Pin TSOP

x4	x8	x16			x16	x8	x4
–	–	VDD	1 •	54	VSS	–	–
NC	DQ0	DQ0	2	53	DQ15	DQ7	NC
–	–	VDDQ	3	52	VSSQ	–	–
NC	NC	DQ1	4	51	DQ14	NC	NC
DQ0	DQ1	DQ2	5	50	DQ13	DQ6	DQ3
–	–	VSSQ	6	49	VDDQ	–	–
NC	NC	DQ3	7	48	DQ12	NC	NC
NC	DQ2	DQ4	8	47	DQ11	DQ5	NC
–	–	VDDQ	9	46	VSSQ	–	–
NC	NC	DQ5	10	45	DQ10	NC	NC
DQ1	DQ3	DQ6	11	44	DQ9	DQ4	DQ2
–	–	VSSQ	12	43	VDDQ	–	–
NC	NC	DQ7	13	42	DQ8	NC	NC
–	–	VDD	14	41	VSS	–	–
NC	NC	DQML	15	40	NC	–	–
–	–	WE#	16	39	DQMH	DQM	DQM
–	–	CAS#	17	38	CLK	–	–
–	–	RAS#	18	37	CKE	–	–
–	–	CS#	19	36	NC	–	–
–	–	BA0	20	35	A11	–	–
–	–	BA1	21	34	A9	–	–
–	–	A10	22	33	A8	–	–
–	–	A0	23	32	A7	–	–
–	–	A1	24	31	A6	–	–
–	–	A2	25	30	A5	–	–
–	–	A3	26	29	A4	–	–
–	–	VDD	27	28	VSS	–	–

Note: The # symbol indicates signal is active LOW. A dash (–) indicates x8 and x4 pin function is same as x16 pin function.

	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0–A9, A11)	1K (A0–A9)	512 (A0–A8)

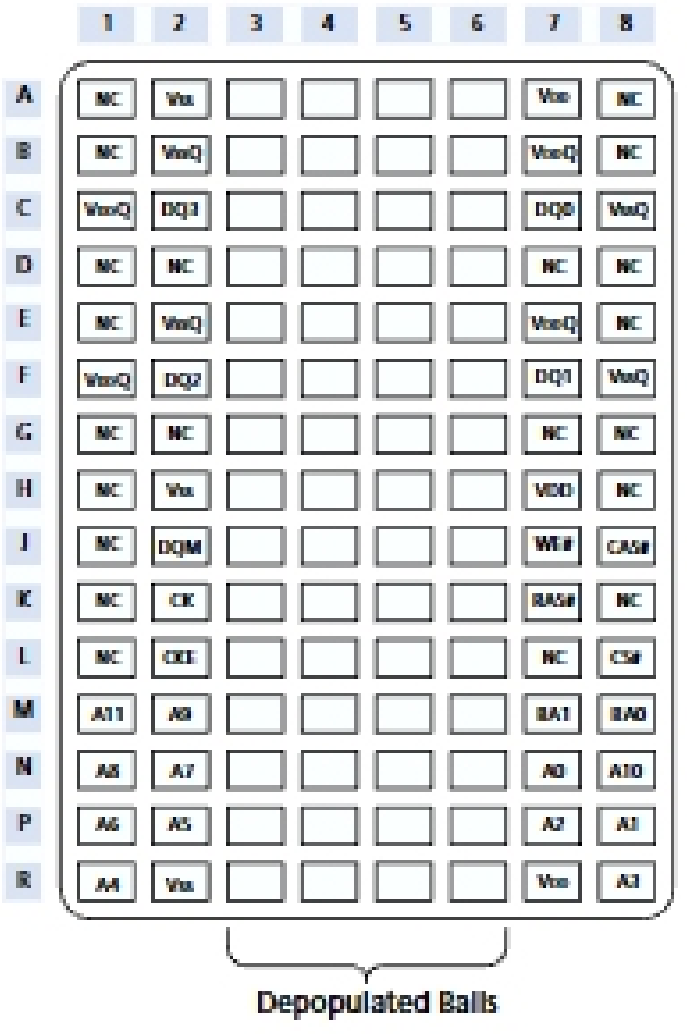
KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 2*	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-7E	143 MHz	–	5.4ns	1.5ns	0.8ns
-7E	133 MHz	5.4ns	–	1.5ns	0.8ns
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-8E[3,4,5]	125 MHz	–	6ns	2ns	1ns
-75	100 MHz	6ns	–	1.5ns	0.8ns
-8E[3,4,5]	100 MHz	6ns	–	2ns	1ns

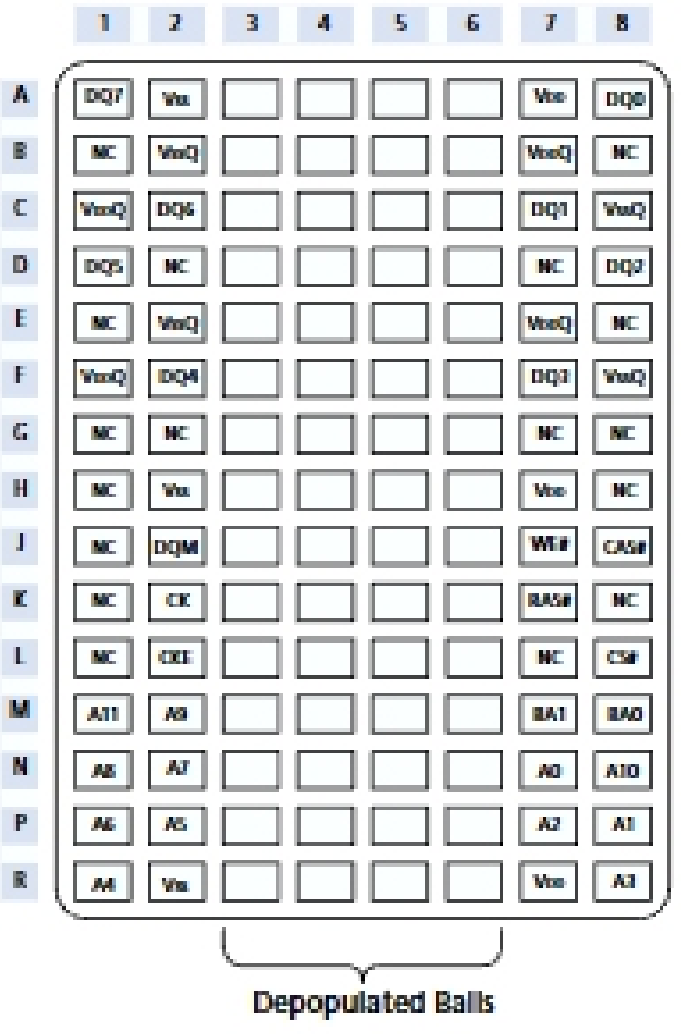
*CL = CAS (READ) latency

FBGA BALL ASSIGNMENT
(Top View)

32 Meg x 4
8 x 16mm and 11 x 13mm



16 Meg x 8
8 x 16mm and 11 x 13mm



128Mb SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC32M4A2TG	32 Meg x 4
MT48LC32M4A2FC*	32 Meg x 4
MT48LC32M4A2FB*	32 Meg x 4
MT48LC16M8A2TG	16 Meg x 8
MT48LC16M8A2FC*	16 Meg x 8
MT48LC16M8A2FB*	16 Meg x 8
MT48LC8M16A2TG	8 Meg x 16

*See page 59 for FBGA Device Marking Table.

GENERAL DESCRIPTION

The Micron® 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 33,554,432-bit banks is organized as 4,096 rows by 2,048 columns by 4 bits. Each of the x8's 33,554,432-bit banks is organized as 4,096 rows by 1,024 columns by 8 bits. Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.