LAB 10: Counters, Clock Dividers, and Debounce Circuits

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Objectives:

In this lab I will learn how to design, implement, test, and synthesize a digital combination lock that can be used on a safe or access-controlled doorway. The combination-lock full state machine will be described in Verilog. A state diagram will be utilized to describe the combination lock FSM, and the switches on the ZYBO board will be used to enter input to the lock. A top level Verilog module will also be created which will drive the counter on the FPGA and then loaded onto the ZYBO board. An XDC file will be used to connect the functions on the top level Verilog module to the ZYBO board. I will learn the concepts and implementation of full state machines. This lab will introduce modern circuit design techniques using Verilog.

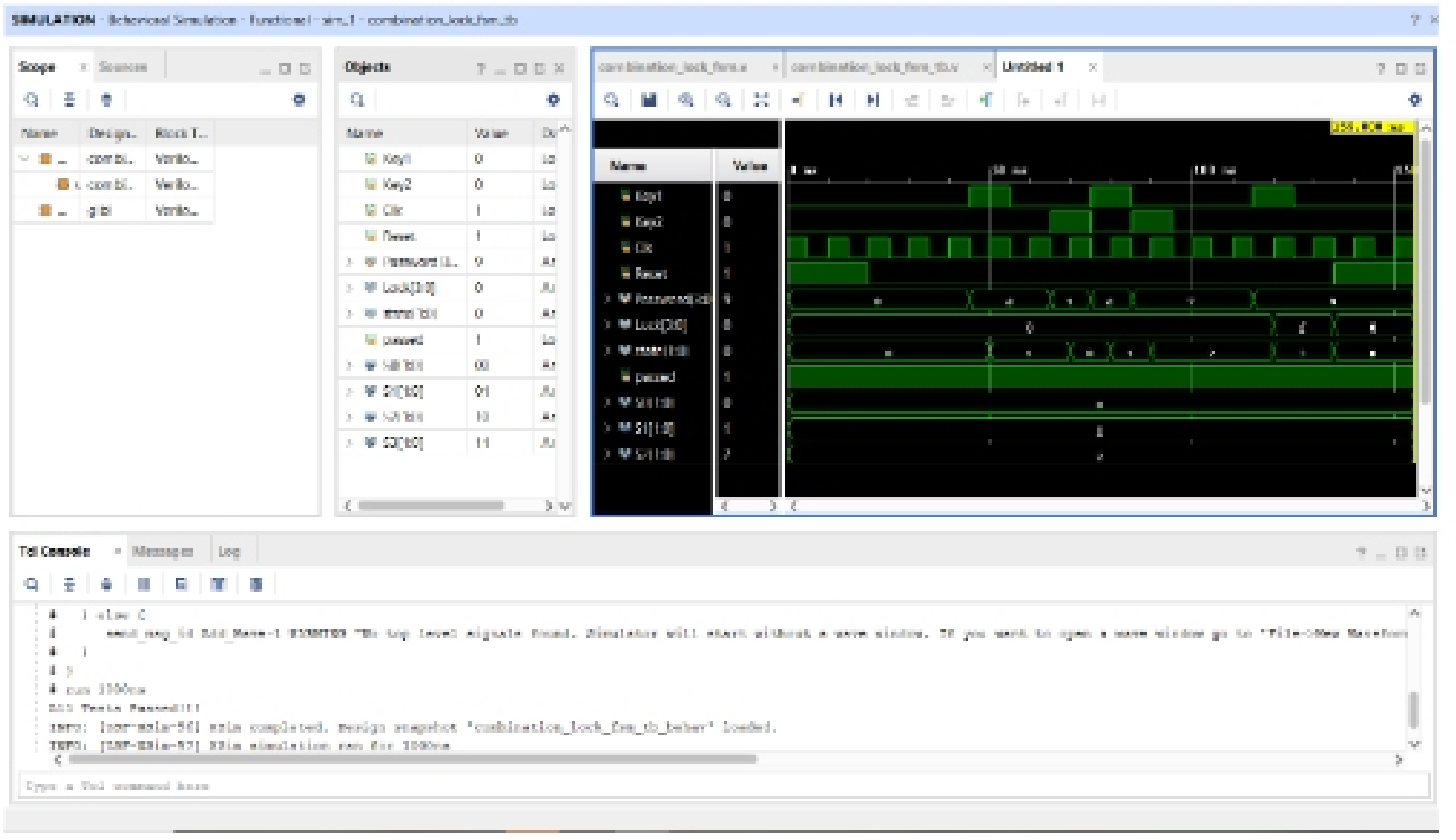
Design:

The objective is to design and implement the digital circuits for a 4 bit, 3 number combination lock FSM, and a 4 bit, 4 number combination lock FSM that can be used on a safe or access-controlled doorway, both described in Verilog. The combination lock FSM will be described using a state diagram system, and then hooked up in combination with a top level Verilog module connected to a series of synchronizers. The synchronizers will be connected to two input keys and the reset button. The top level Verilog module will drive the counter on the FPGA and then will be loaded onto the ZYBO board. The switches on the ZYBO board will be used to enter input to the lock. An XDC file will be used to connect the functions on the top level Verilog module to the ZYBO board. Both designs will be synthesized and implemented onto the ZYBO board and tested for functionality on the board. All 4 LEDs will light up if the password is inputted correctly.

Results:

All the Verilog modules functioned as expected. The final top level up counter module worked and functioned without issue, after much debugging. They were tested against test benches and simulated the circuit without fault. All the modules were simulated using behavioral and structural Verilog. The synthesis and implementation of both 3 and 4 number combination locks on the ZYBO board had functional keys and reset buttons, and would only light up when the proper sequence of numbers and keys were inputted.

Combination Lock FSM



Conclusion:

In this lab I created simple behavioral Verilog modules for a 4 bit, 3 number combination lock FSM, and a 4 bit, 4 number combination lock FSM that can be used on a safe or access-controlled doorway, both described in Verilog. The combination lock FSM was described using a state diagram system, and then hooked up in combination with a top level Verilog module connected to a series of synchronizers. The base modules functioned correctly. All Verilog modules were tested with a test bench simulation to error check and debug. The synthesis and implementation of the combination lock on the ZYBO board had functional keys and reset buttons, and used the switches on the board to input the password in binary. The lock would only light up if all numbers were inputted correctly with the correct key inputs. In this lab I learned modern behavioral circuit design techniques using Verilog, the concepts and implementation of Full State machines, and descriptions in verilog using a state diagram.

Questions:

1. Include the source code with comments for all modules you simulated and/or implemented in lab. You do not have to include test bench code that was provided! Code