

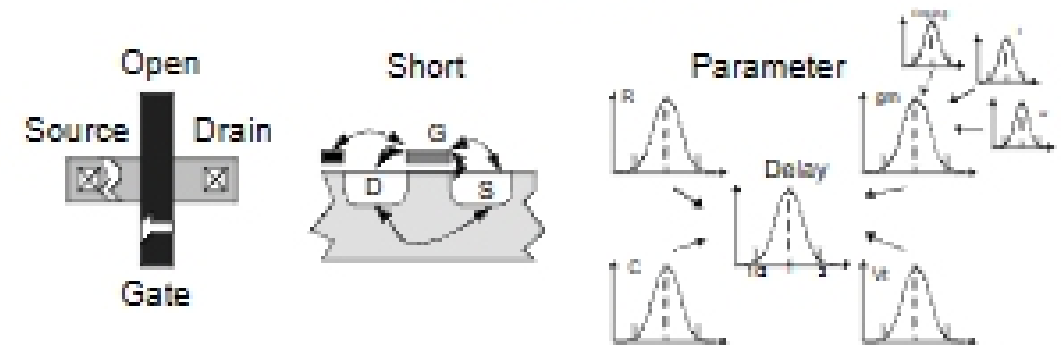
Lecture 37: Testing

- Fault models
- Test Combinational circuits
- Test Sequential circuits

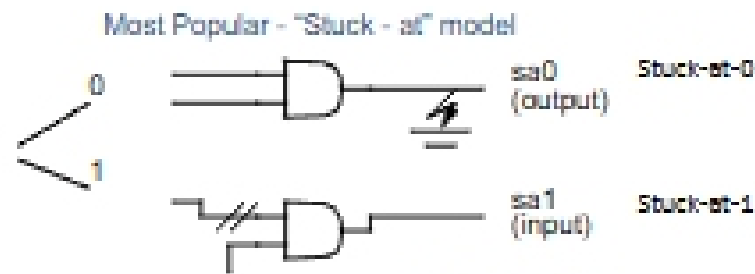
Defect and Faults

Fault types: Functional.
Timing.

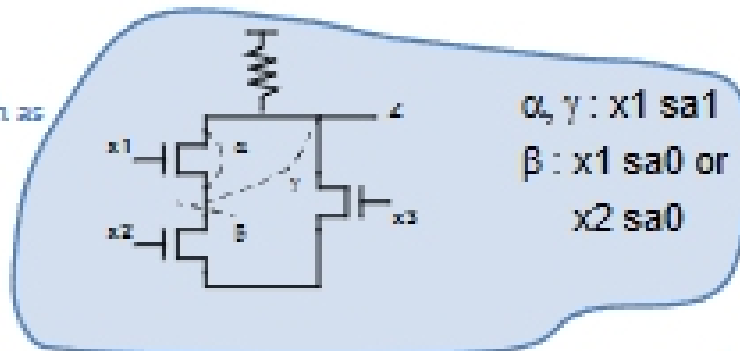
Abstraction level: Transistor. (layout)
Gate. (netlist)
Macro (functional blocks).



Logical-level fault model



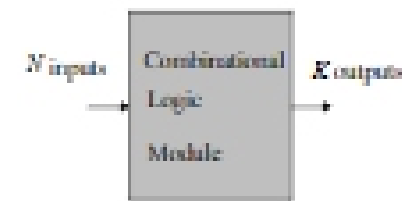
Covers many other occurring faults, such as opens and shorts.



Testing Approaches

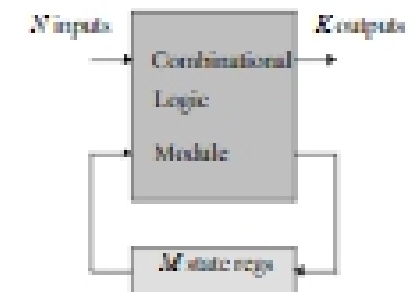
1. Exhaustive Algorithm

- For n -input circuit, generate all 2^n input patterns
- Infeasible, unless circuit has < 20 inputs



(a) Combinational function

2^N patterns



(b) Sequential engine

2^{N+M} patterns

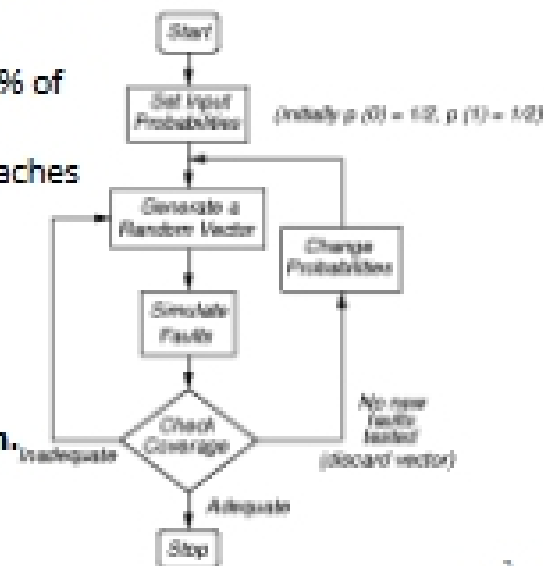
Testing Approaches

2. Random Pattern Generation

- Flow chart for method
- Use to get tests for 60-80% of faults, then switch to D-algorithm or other approaches for the rest

Q: How to estimate fault coverage?

A: Through Fault Simulation.

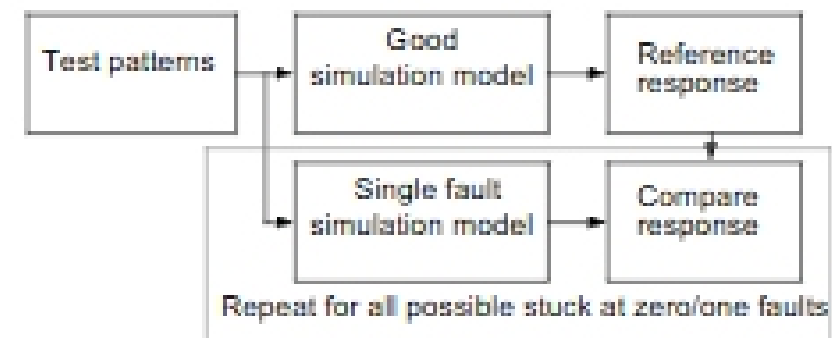


3/14/2014

2

Fault Simulation

Fault coverage found by fault simulations



Requires long simulation times !

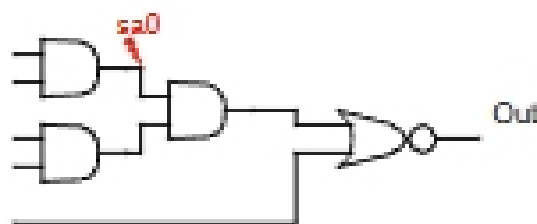
Toggle test (counts how many times each node has changed) can be used to get a first impression of fault coverage.

3/14/2014

3

Fault Simulation

- **Basic Terms:**
 - **Controllability:** the ease of controlling the state of a node
 - **Observability:** the ease of observing the state of a node
- **Goal:** determine input pattern that
 - makes a fault controllable (triggers the fault)
 - makes its impact visible at the output nodes

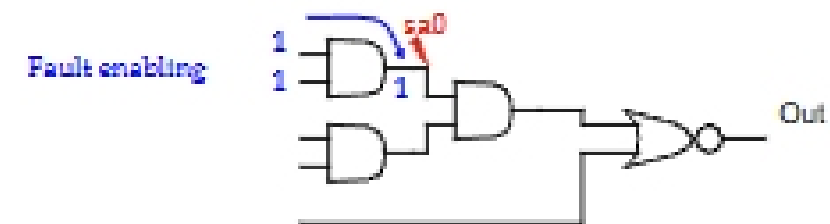


3/14/2014

7

Fault Simulation

- **Basic Terms:**
 - **Controllability:** the ease of controlling the state of a node
 - **Observability:** the ease of observing the state of a node
- **Goal:** determine input pattern that
 - makes a fault controllable (triggers the fault)
 - makes its impact visible at the output nodes



3/14/2014

8

Fault Simulation

- **Basic Terms:**
 - **Controllability:** the ease of controlling the state of a node
 - **Observability:** the ease of observing the state of a node
- **Goal:** determine input pattern that
 - makes a fault controllable (triggers the fault)
 - makes its impact visible at the output nodes



Technique Used: D-algorithm

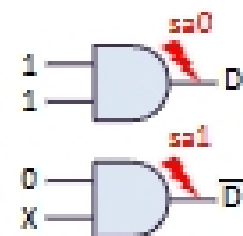
D-algorithm

- Models circuit faults
 - Stuck-at-0
 - Stuck-at-1
- 5-Value Logic
 - 0 – binary 0 in both good and fault circuit
 - 1 – binary 1 in both good and fault circuit
 - X – don't care
 - \overline{D} – binary 1 in good circuit, 0 in bad circuit
 - $\overline{\overline{D}}$ – binary 0 in good circuit, 1 in bad circuit

D-algorithm

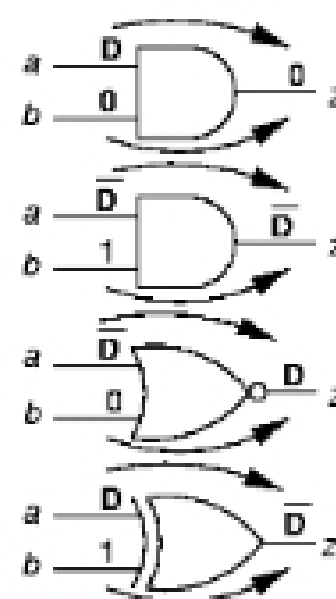
- **Primitive D-Cube** of Failure

- AND Output sa0: "1 1 \overline{D} "
- AND Output sa1: "0 X $\overline{\overline{D}}$ "
or "X 0 $\overline{\overline{D}}$ "
- Wire sa0: " \overline{D} "



- **Propagation D-cube** – models conditions under which fault effect propagates through gate

Forward Implication



- Results in logic gate inputs that uniquely determine the output

- AND gate forward implication table:

a \ b	0	1	X	\overline{D}	$\overline{\overline{D}}$
0	0	0	0	0	0
1	0	1	X	\overline{D}	$\overline{\overline{D}}$
X	0	X	X	X	X
\overline{D}	0	\overline{D}	X	\overline{D}	0
$\overline{\overline{D}}$	0	$\overline{\overline{D}}$	X	0	$\overline{\overline{D}}$