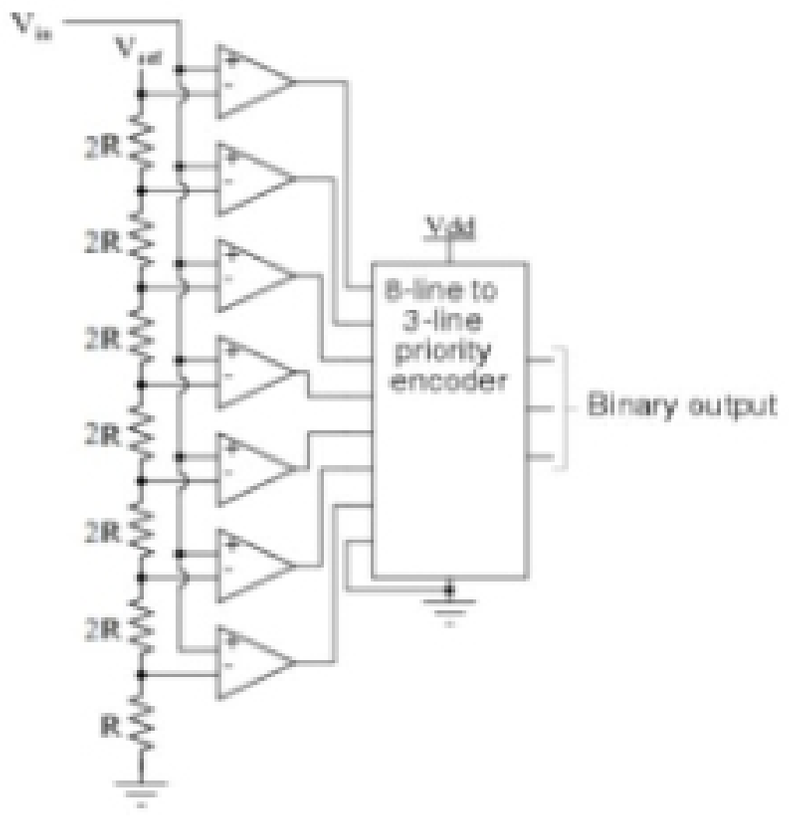
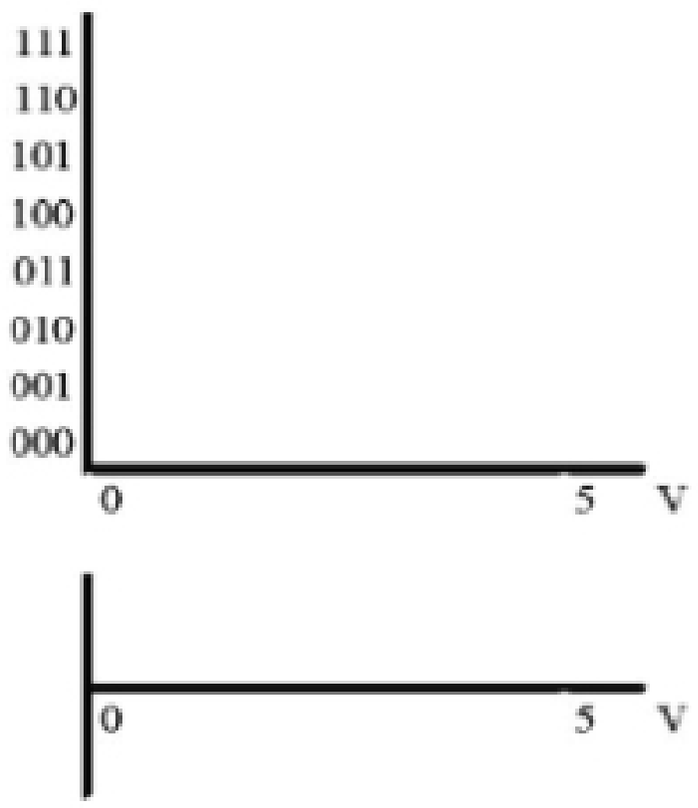
CPEG 222 Spring 2014

Homework 3

Due May 8 at noon (through sakai)
Note: To receive full credit, please show your steps and put comments for your code.

1. Consider the following 3-bit ADC. Draw the conversion transfer function (binary output vs input voltage) on the top graph. Draw the quantization error transfer function (error voltage vs input voltage) on the bottom graph. Assume Vref is 5V.





2. Assume that a sensor outputs an analog signal with a range of 0V and 4V (i.e., reference voltage = 4V). A linear A/D converter then converts the analog signal into a digital signal. The transfer function is shifted to the left ½ LSB to reduce quantization error.

   (a) Identify the smallest detectable change in voltage (*that is, no matter what the original voltage is, the change can always be detected*) if the ADC uses (1) 4-bits of resolution; (2) 7-bits of resolution.
   (b) For an input voltage of 3.14V, identify the quantization error if the ADC uses (1) 4-bits of resolution; (2) 7-bits of resolution.
   (c) Assume the A/D converter supplies samples at 40 kHz. When a sample arrives, an interrupt handler will be invoked to process the sample and feed the result to the application. The ADC ISR executes 150 instructions to process each sample for the application. The processor is 40MHz, and executes one instruction per cycle. Assuming the processor is running only the application and interrupt handler, how many application instructions can be executed between two consecutive interrupts?

3. Imagine that you want to attach an LED to the ARM Advanced Peripheral Bus (APB). Sketch out the glue logic needed to interface a D flip-flop (DFF) to the APB. Assume that the PSEL line is the peripheral select (i.e. it goes high when the processor is addressing the DFF) and that the DFF will be attached to data bits PWDATA[0] and PRDATA[0] (through tri-state drivers). You should be able to change the value of the DFF by writing the memory location corresponding to the PSEL and read the current value of the DFFs by reading the location. Assume that the DFF has an enable (ENA) line that, when not asserted, ignores any inputs (e.g. D and CLK) but continues to drive Q and Q'. The

APB signals available to you are: PCLK, PADDR, PWRITE, PSEL, PENABLE, PWDATA, and PRDATA.

4. Direct Memory Access (DMA) allows devices to access memory directly rather than working through the CPU. This can dramatically speed-up the performance of peripherals, but adds complexity to memory system implementations. Of the following peripherals, which would benefit from DMA? What criteria determine if DMA is appropriate?
   (a) Graphics card
   (b) Sound card

5. A 7-bit Hamming code consists of 3 parity bits and 4 data bits. The 3 parity bits are used to correct single bit error, regardless of whether the error occurs in the data or in the parity bits.

Position	7	6	5	4	3	2	1
Bit	d_3	d_2	d_1	p_2	d_0	p_1	p_0

$$p_2 = d_3 \oplus d_2 \oplus d_1$$
$$p_1 = d_3 \oplus d_2 \oplus d_0$$
$$p_0 = d_3 \oplus d_1 \oplus d_0$$

   (a) Are the following two codes valid Hamming codes? If any of them is not valid, which bit has an error?
   0110100
   0101100
   (b) We know that the parity value for the data value 0100 is 110. Please identify the two codewords that have the complementary parity value of **001**.
   (c) Prove that the Hamming distance of the 7-bit Hamming code is 3.