Lab 3: Logic Minimization with Karnaugh Maps

Jacob Pantalone

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TA: Ye Wang

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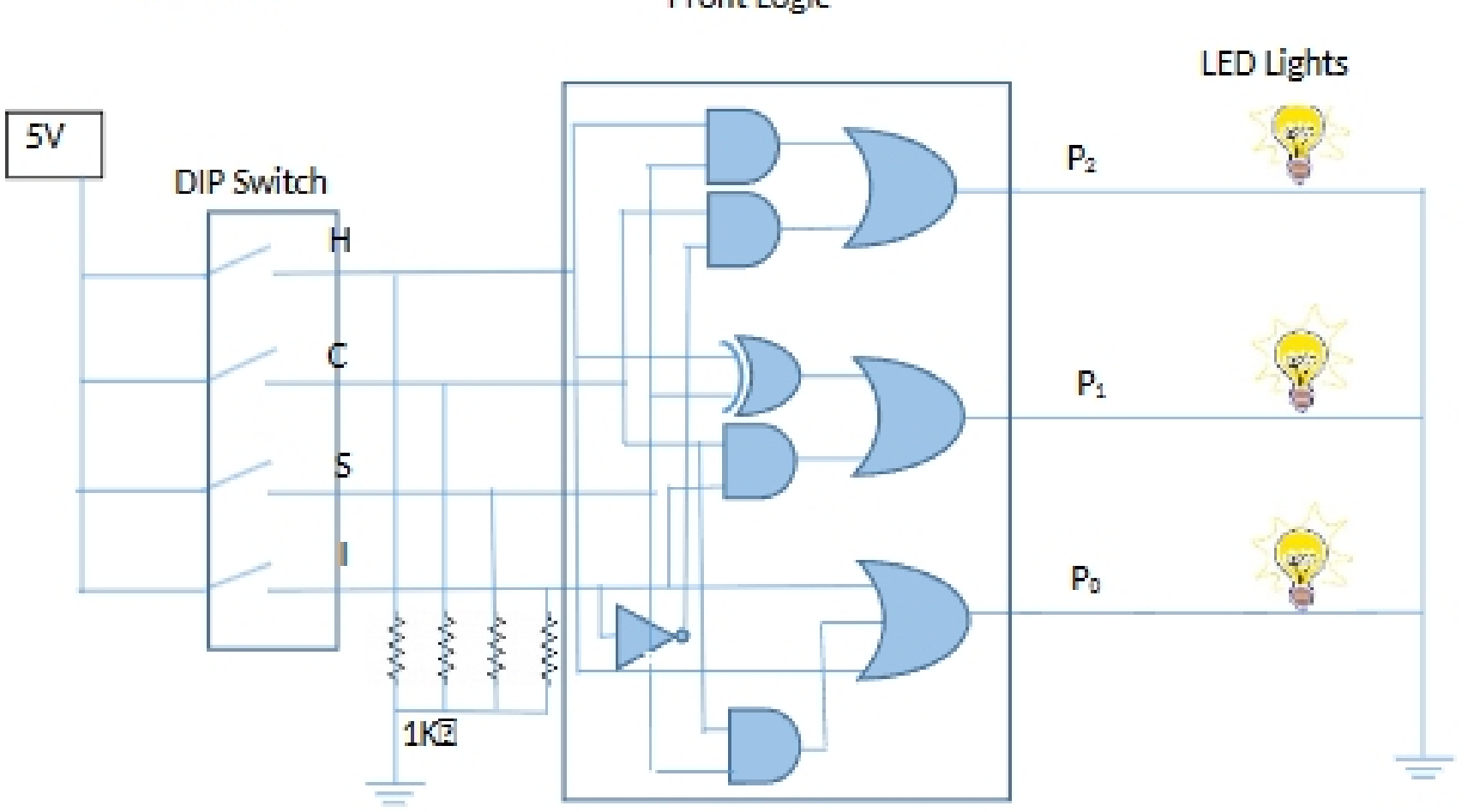
Objectives:

The purpose of this week's lab assignment is to introduce a real-world application of digital electronics while demonstrating the use of Karnaugh-Maps for logic minimization. In the laboratory, I will breadboard a simple circuit which calculates the profits of a small farm. I will also feed the output of your circuit into a seven-segment display for ease of viewing.

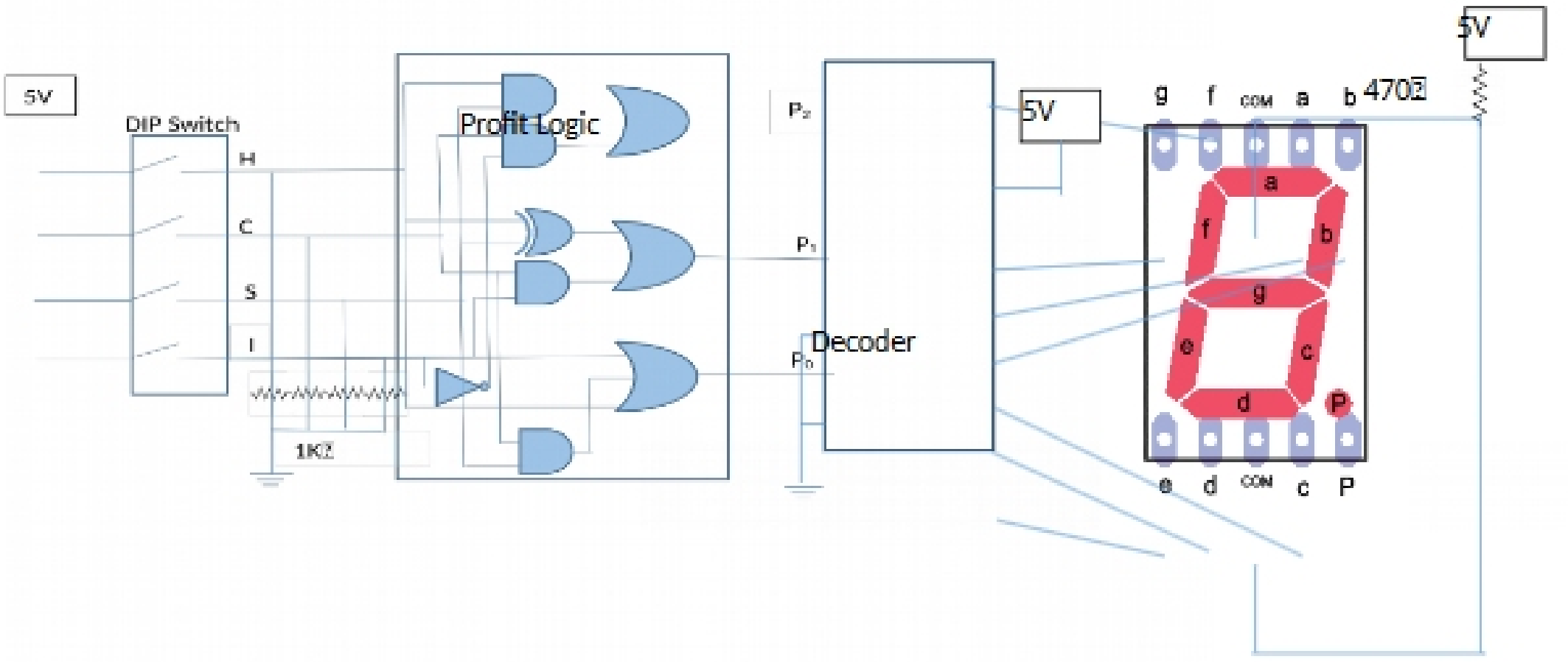
Design 1:

Having a constant power supply of 5V, the Vcc is then attached to four ports on the DIP switch so that we can simulate the different possibile inputs of the profit calculator. On the other side of the dipswitch, wire the inputs to ground with a 1kΩ resister. The inputs are then attached to the profit logic, which generates the outputs P_2, P_1, and P_0. P_2 should use two AND (74ALS08) gates and an OR (74ALS32) gate as shown in the diagram, P_1 needs an XOR (SN74ALS86), AND, and an OR gate in the sequence depicted below, and P_0 requires a NOT (74ALS04), AND, and an OR gate as shown. These are then wired to the LED lights to determine the binary numbers.



Design 2:

Continuing from the first design, you must remove the LED lights and instead, wire the oputputs to the decoder (SN74LS47). P_0 goes to port A, P_1 goes to port B, and P_2 goes to port C. Be sure to wire port D and the GND port to ground and the VCC port to the 5V line. You then must wire the decoder to the 7-segment display. Port f goes to port 9, port g goes to port 10 port a goes to port 7, port b goes to port 6, port e goes to port 1, port d goes to port 2, and port c goes to port 4. Finally, connect the com ports on the 7-segment display to the 5V line with a 470Ω resister.



Decoder (SN74AL547)