Lab 3. Adding a Custom Hardware IP, and interfacing it with Software

Objective

In this lab, we will add a Custom hardware IP (a user-defined Verilog block), which will be implemented on the FPGA and interface it to the software running on the PowerPC.

- A Custom IP (Verilog code) is used to implement a multiplier. The Verilog code reads the values from two registers (say R1 and R2) and writes the multiplied output to a third register (R3).
- Software is used for testing the multiplier. The software code will write values to registers R1 and R2, read the multiplication result from R3, and display the values of R1, R2 and R3 on a hyperterminal screen.

Overview

Create a Base System (or use the one created in Lab 2) consisting of a PowerPC, RS232 interface and a PLB BRAM. In this lab, we will add a Custom IP – which will multiply 2 32-bit numbers stored in 2 registers and write the result to a third register.

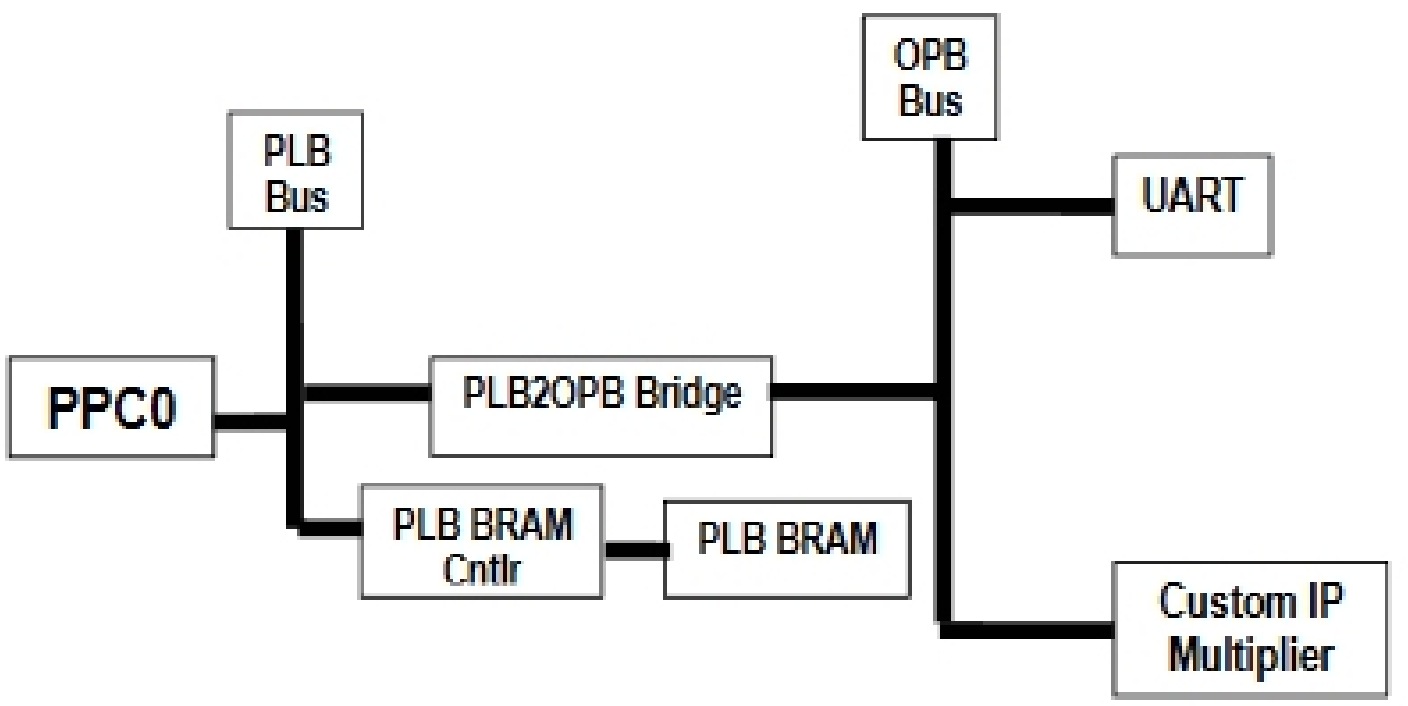

Figure 1. Complete System

Procedure

Copy the base system created in Lab 2 or create a new base system in a directory called lab3.

After the design is setup using the Base System Builder (BSB), add the Custom IP using the following steps.

1. Under the Hardware tab, select 'Create/Import Peripheral'.
   Click Next on the Welcome window. Select 'Create templates for a new peripheral'. Click Next.

In the Repository or Project window, select 'To an XPS project' and browse to the directory where your directory Lab3 is located. Click Next.

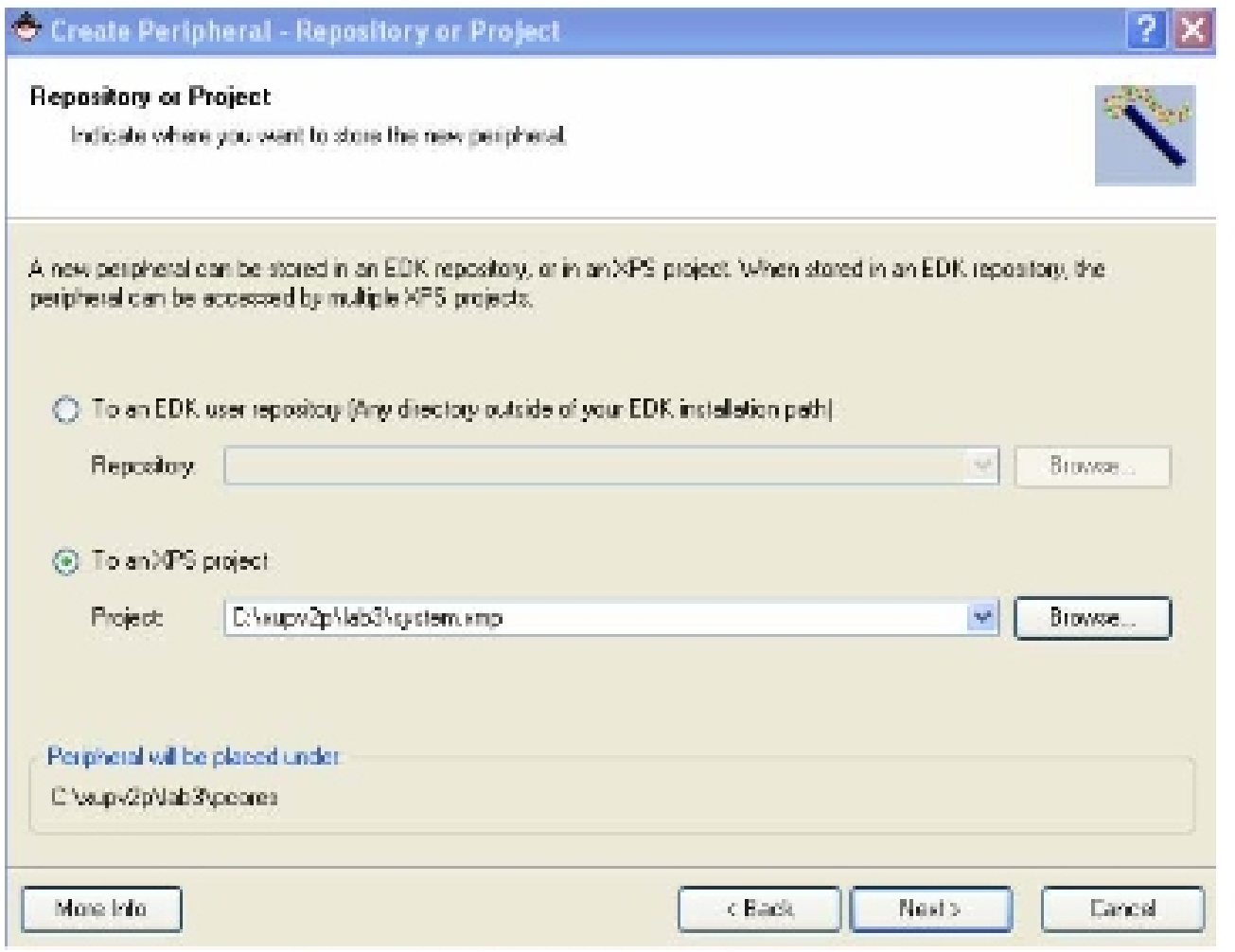

Figure 2.Create/ Import Peripheral

2. Name the new peripheral 'multiply' (this will be the name of your Verilog module). The rest of the settings remain unchanged. Click Next.

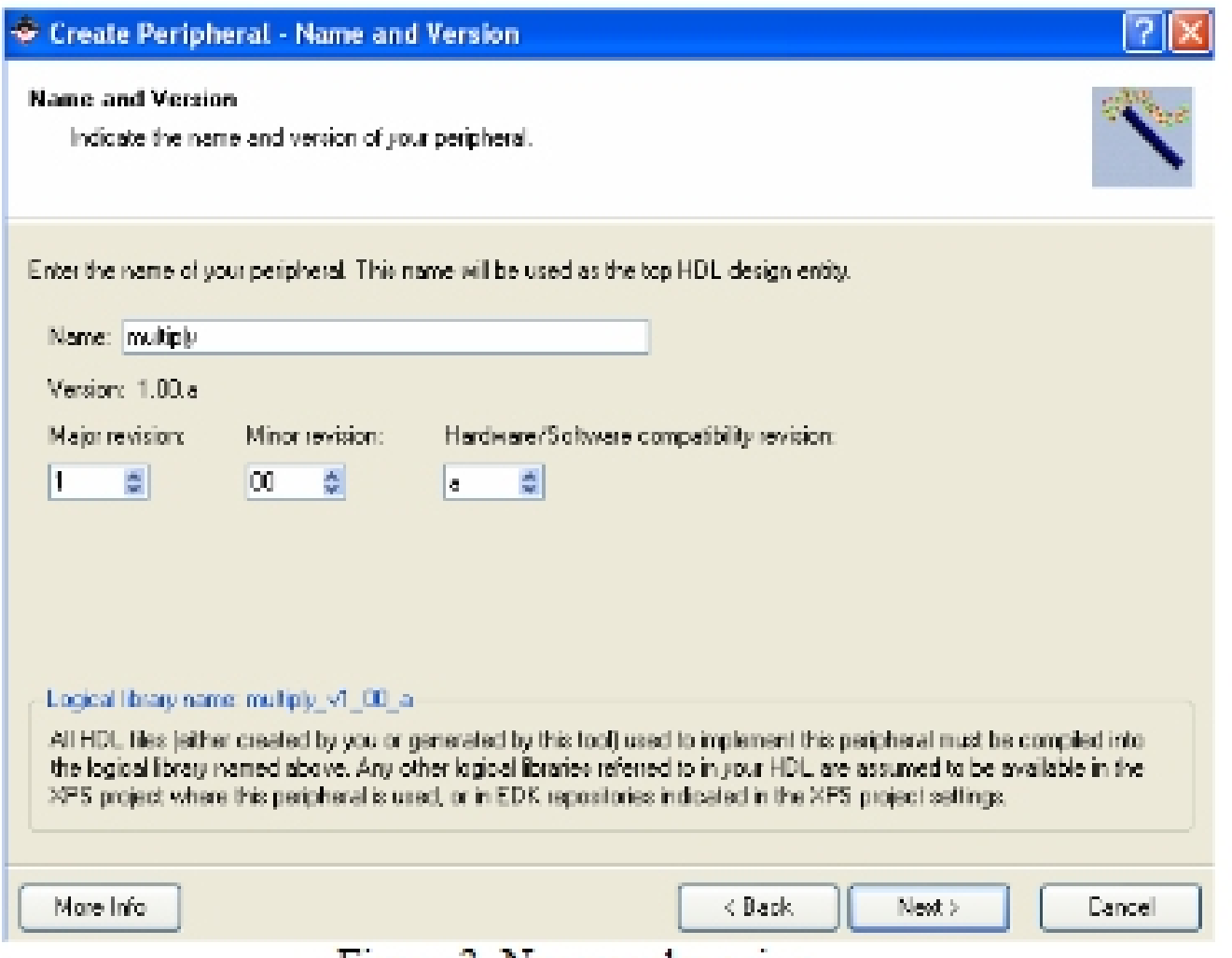

Figure 3. Name and version

3. Now, the Bus Interface Window will open. We want to connect the IP to the On-chip Peripheral Bus (OPB). Select OPB and click Next.
   In the IPIF Services window, check 'User logic S/W register support'. Our custom IP will interface with the software using these software registers. Click Next.

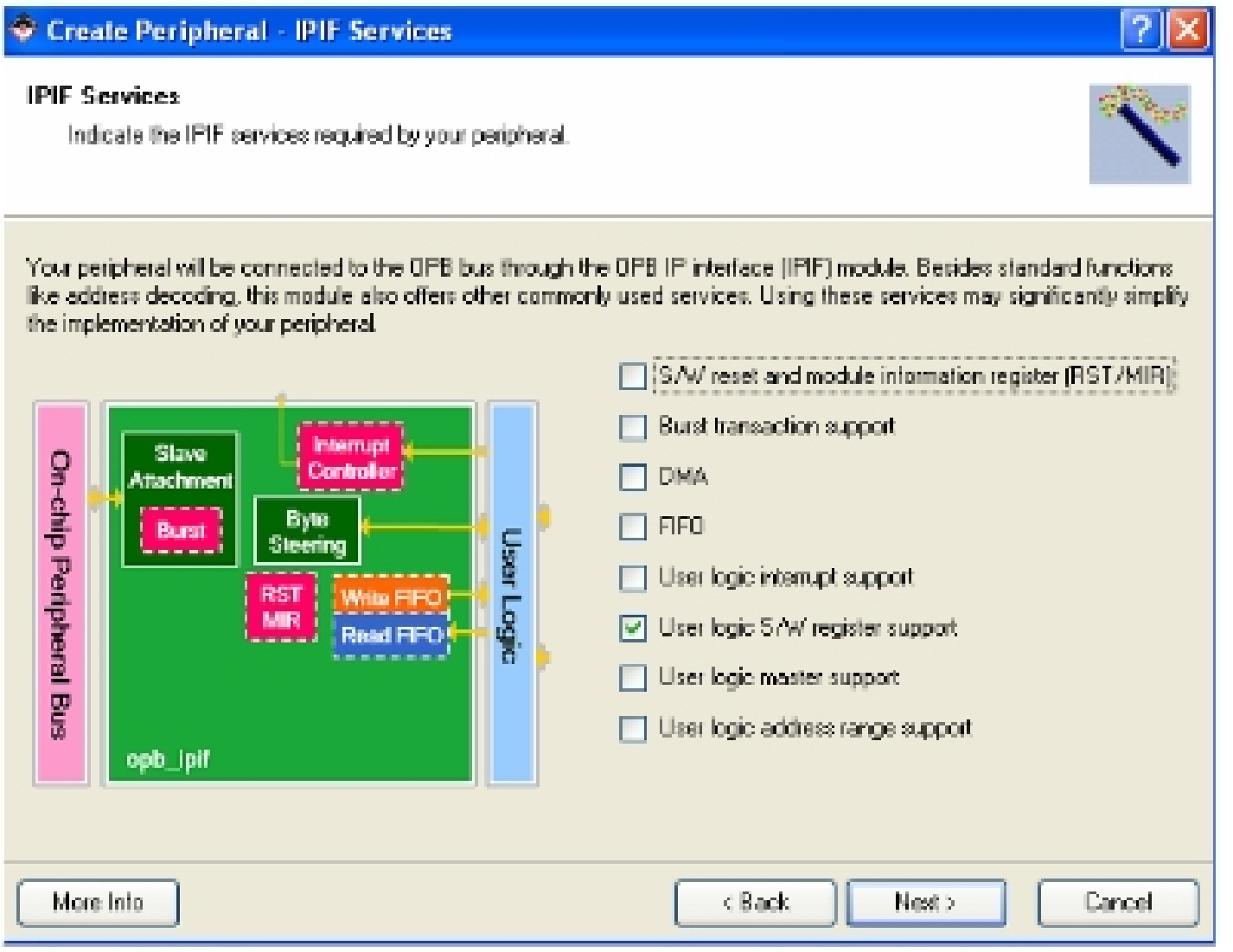

Figure 4. IPIF Services

4. In the User S/W Register window, set the 'Number of software accessible registers' to 3, and set 'Data width' of each register to 32. We need two 32-bit registers to hold the numbers to be multiplied, and a third 32-bit register to hold the multiplication result.
   Note that we can only specify the register widths to be identical. When we use the 'Multiply' IP, we will ensure that the multiplier and multiplicand are 16 bit values. Click Next.

5. In the IP Interconnect (IPIC) window, some ports are selected by default for the custom IP. These ports are used for communication between the user logic and OPB bus. Accept the default setting and click Next.

6. In the window that shows up next, uncheck 'Generate BFM simulation platform for ModelSim-SE or ModelSim-PE'. We do not need the simulation support for this exercise. Click Next.